Introduction to Modern Signal Generation; from Analog to Digital: Needs, Advantages, Disadvantages and "Solutions"

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Incentives:

In the age of wideband modulation capabilities, our “good old” signal generators maybe nice and low noise, but unable to generate the needed modern signals. On the other hand they are a good starting topic to explain the circuitry of analog signal generators, even their complexity and how and why modern signal generators evolved. This also needs an introduction to frequency synthesis.

The traditional communication essentially took place from point to point and starting with AM modulation, for broadcast later with FM modulation, evolved to single side-band suppressed carrier modulation (SSB). For the most reliable communication, MORSE code was invented and in many ways is still used and actually the forerunner of digital modulation. To assess today’s problems here is an introductory chapter of what really happens. [1-6]

The Radio Channel and Modulation Requirements

Introduction

The transmission of information from a fixed station to a mobile is considerably influenced by the characteristics of the radio channel. The RF signal arrives at the receiving antenna not only on the direct path but is normally reflected by natural and artificial obstacles in its way. Consequently the signal arrives at the receiver several times in the form of echoes which are superimposed on the direct signal. (See Figure: 1). This superposition may be an advantage as the energy received in this case is greater than in single-path reception. This feature is made use of in the DAB single-frequency network. However, this characteristic may be a disadvantage when the different waves cancel each other under unfavorable phase conditions. In conventional car radio reception this effect is known as fading. It is particularly annoying when the vehicle stops in an area where the field strength is reduced because of fading (for example, at traffic lights). Additional difficulties arise when digital signals are transmitted. If strong echo signals (compared to the directly received signal) arrive at the receiver with a delay in the order of a symbol period or more, time-adjacent symbols interfere with each other. In addition, the receive frequency may be falsified at high vehicle speeds because of the Doppler effect so that the receiver may have problems to estimate the instantaneous phase in the case of angle-modulated carriers. Both effects lead to a high symbol error rate even if the field strength is sufficiently high. Radio broadcasting systems using conventional frequency modulation are hardly affected by these interfering effects. If an analog system is replaced by a digital one which is expected to offer advantages over the previous system, it has to be ensured that these advantages--for example, better AF S/N and the possibility to offer supplementary services to the subscriber--are not at the expense of reception in hilly terrain or at high vehicle speeds because of extreme fading.

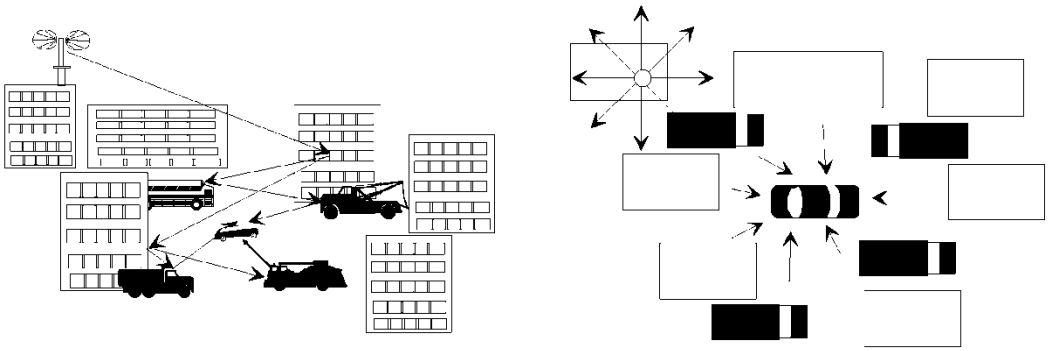


Figure 1: Mobile receiver affected by fading [1]

For this reason a modulation method combined with suitable error protection has to be found for mobile reception in a typical radio channel, which is immune to fading, echo and Doppler effects.[1]

With a view to this, more detailed information on the radio channel is required. The channel can be described by means of a model. In the worst case, which may be the case for reception in built-up areas, it can be assumed that the mobile receives the signal on several indirect paths but not on a direct one. The signals are reflected for example by large buildings; the resulting signal delays are relatively long. In the vicinity of the receiver these paths are split up into a great number of subpaths; the delays of these signals are relatively short. These signals may again be reflected by buildings but also by other vehicles or natural obstacles like trees. Assuming the subpaths being statistically independent of each other, the superimposed signals at the antenna input cause considerable time- and position-dependent field-strength variations with an amplitude obeying the Rayleigh distribution (Figures 2 and 3).[1]

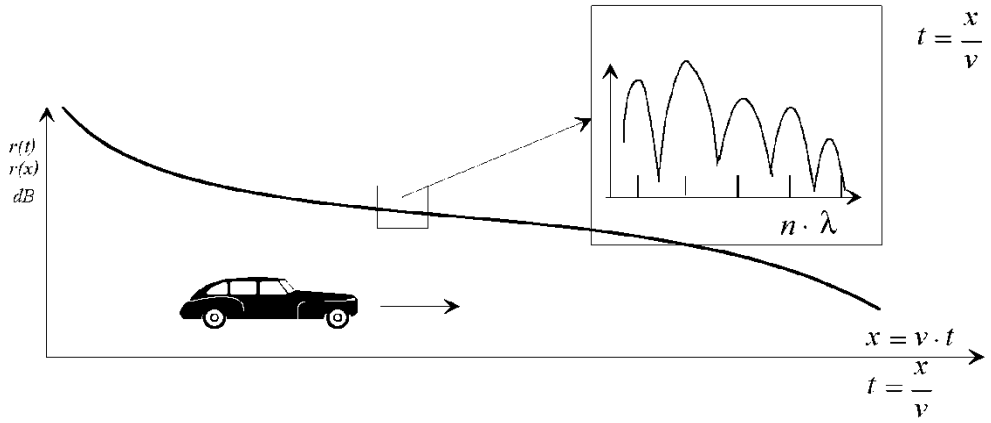


Figure 2: Receive signal as a function of time or position [1]

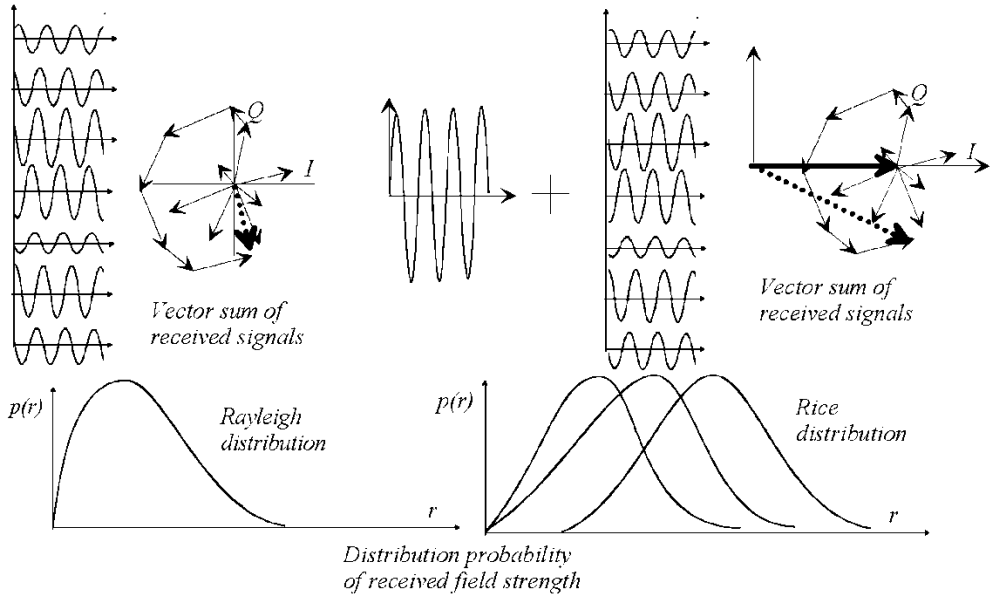


Figure 3: Rayleigh and Rice distribution [1]

If a direct path is received in addition, the distribution changes to the Rice distribution and finally, when the direct path becomes dominant, the distribution follows the Gaussian distribution with the field strength of the direct path being used as the center value.

In a Rayleigh channel the bit error rate increases dramatically compared to the BER in an AWGN channel produces (Figure 4).

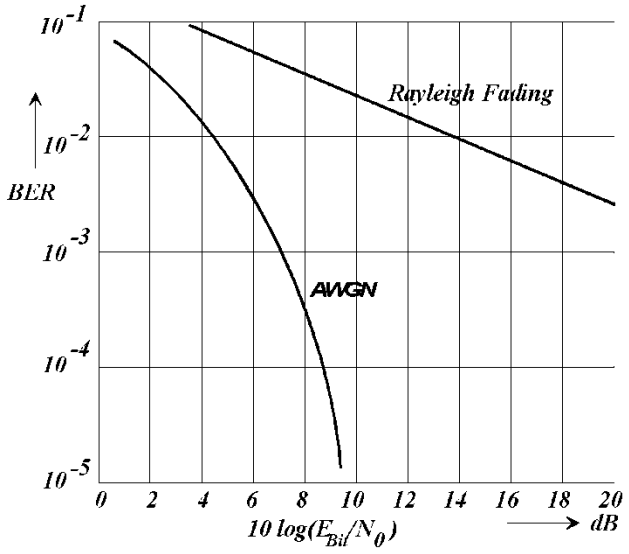


Figure 4: BER in a Rayleigh channel [1]

Channel Impulse Response

This scenario can be demonstrated by means of the channel impulse response. Let's assume that a very short pulse of extremely high amplitude (in the ideal case a Dirac pulse $\delta(t)$) is sent by the transmitting antenna at a time $t_0 = 0$. This pulse arrives at the receiving antenna direct and in the form of reflections with different delays τ_i and different amplitudes because of path losses. The impulse response of the radio channel is the sum of all received pulses (Figure 5). Since the mobile receiver and also some of the reflecting objects are moving, the channel impulse response is a function of time and of delays τ_i; that is, it corresponds to

$$h(t,\tau) = \sum_N a_i \delta(t - \tau_i) \tag{1}$$

This shows that delta functions sent at different times *t,* causes different reactions in the radio channel.

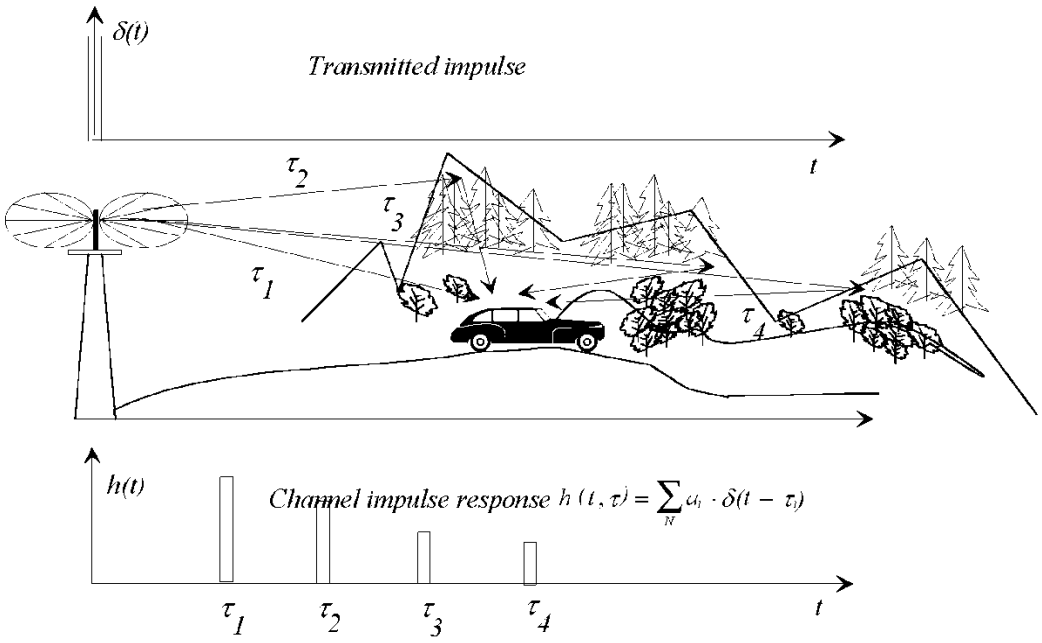


Figure 5: Channel impulse response [1]

In many experimental investigations different landscape models with typical echo profiles were created.

The most important are:

- rural area (RA)
- typical urban area (TU)
- bad urban area (BA)
- hilly terrain (HT)

The channel impulse response informs on how the received power is distributed to the individual echoes. A parameter, the "delay spread" can be calculated from the channel impulse response, permitting an approximate description of typical landscape models (Figure 6).[1]

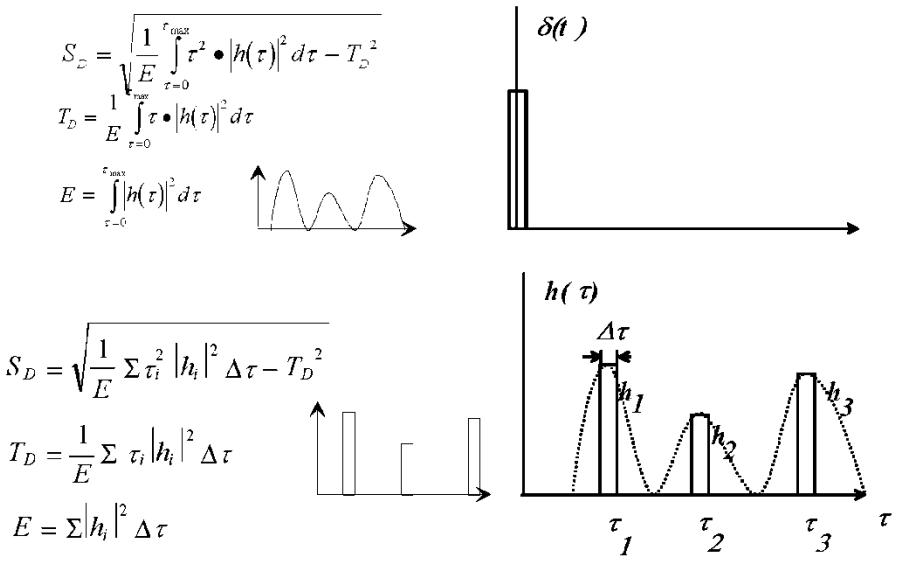


Figure 6: Calculation of delay spread [1]

The delay spread also roughly informs on the modulation parameters carrier frequency, symbol period and duration of guard interval, which have to be selected in relation to each other. If the receiver is located in an area with a high delay spread (for example, in hilly terrain), echoes of the symbols sent at different times are superimposed when broadband modulation methods with a short symbol period are used. In the case of DAB, this problem is aggravated by the use of single-frequency networks. An adjacent transmitter emitting the same information on the same frequency has the effect of an artificial echo (Figure 7).[1]

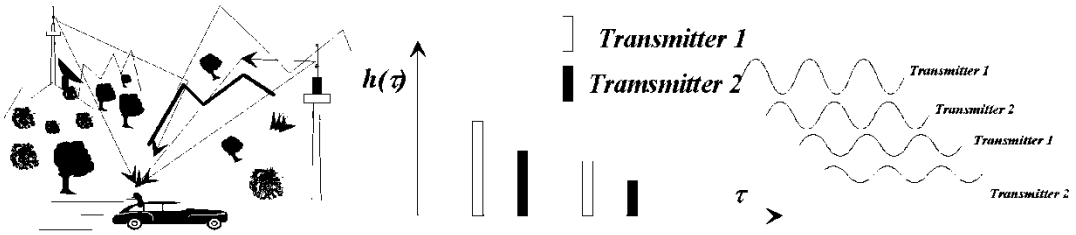


Figure 7: Artificial and natural echoes in the single-frequency network [1]

A constructive superposition of echoes is only possible if the symbol period is much greater than the delay spread. The following holds:

$$T_s > 10T_d \tag{2}$$

This has the consequence that relatively narrowband modulation methods have to be used. If this is not possible, channel equalizing is required.

For the channel equalizing a continuous estimation of the radio channel is necessary. The estimation is performed with the aid of a periodic transmission of data known to the receiver. In networks according to the GSA standards a mid-amble consisting of 26 bits--the training sequence--is transmitted with every burst. The training sequence corresponds to a characteristic pattern of I/Q signals that is kept in a memory in the receiver. The baseband signals of every received training sequence are correlated with the stored ones. From this correlation the channel can be estimated, the properties of the estimated channel will then be fed to the equalizer (Figure 8).

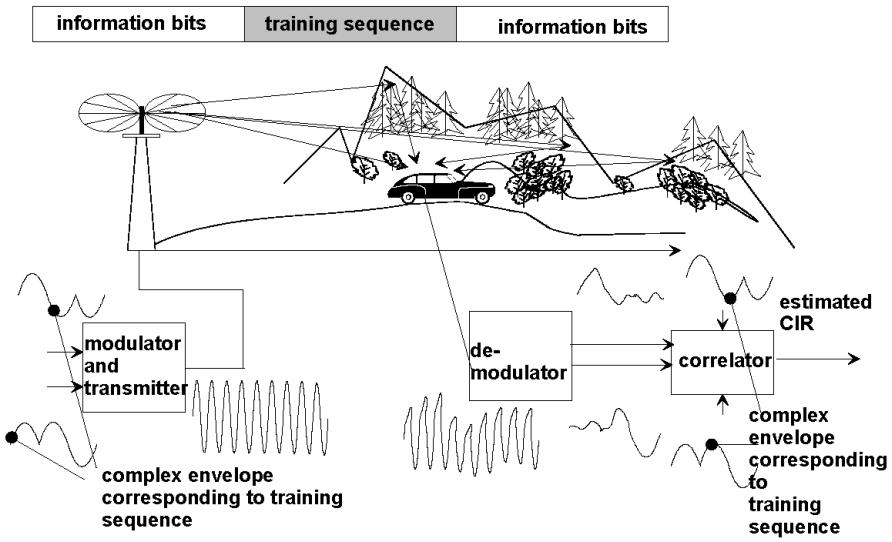


Figure 8: Channel Estimation [1]

The equalizer uses the Viterbi algorithm (maximum sequence likelihood estimation) for the estimation of the phases which most likely have been sent at the sampling times. From these phases the information bits are calculated (Figure 9). A well designed equalizer then will superimpose the energies of the single echoes constructively, so that the result in an area, where the echoes are not too much delayed, delay times up to 16 μs have to be tolerated by a receiver, are better than in an area with no significant echoes (Figure 10).

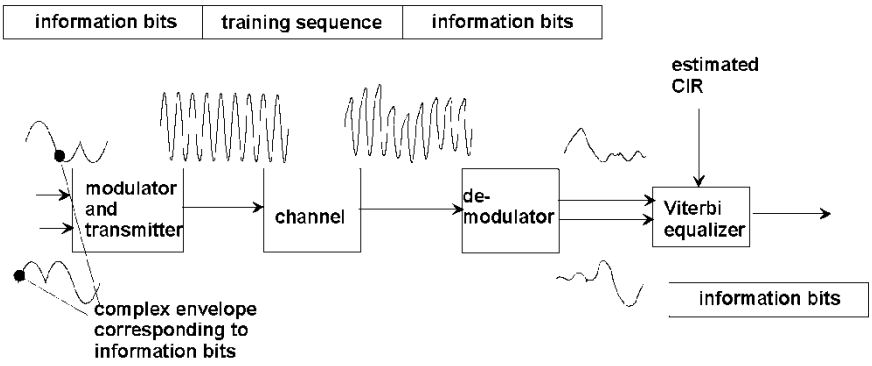


Figure 9: Channel equalization [1]

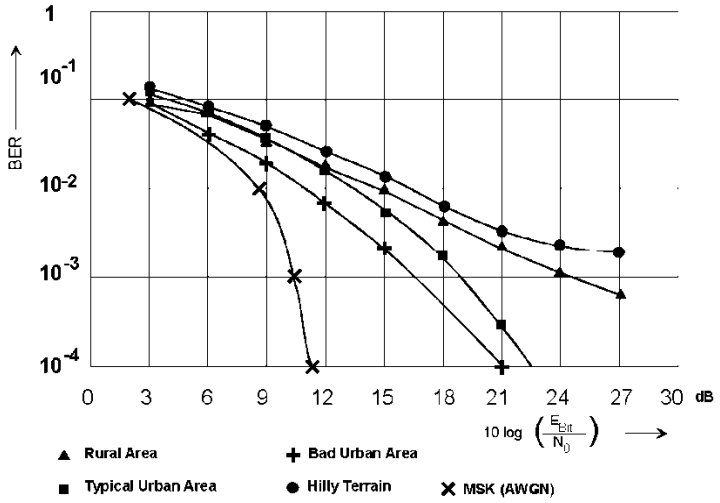


Figure 10: BERs after the channel equalizer in different areas [1]

Remaining bit errors are eliminated using another Viterbi decoder for the at the transmitter convolutionally encoded data sequences.

The ability of a mobile receiver to work in a hostile environment such as the radio channel with echoes must be proven. The test is performed with the aid of a fading simulator. The fading simulator simulates different scenarios with different delay times and different Doppler profiles. A signal generator generates undistorted I/Q modulated RF signals which are downconverted into the baseband. Here the I/Q signals are digitized and split into different channels where they are delayed and attenuated and where Doppler effects are superimposed. After combination of these distorted signals at the output of the baseband section of the simulator these signals modulate the RF carrier which is the test signal for the receiver under test (Figure 11).

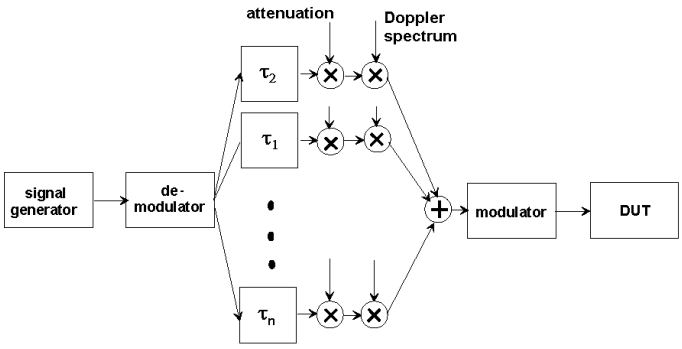


Figure 11: Fading simulator [1]

To make the tests comparable GSM recommends typical profiles; for example:

- Rural Area (RAx)
- Typical Urban (TUx)
- Hilly Terrain (HTx)

where number and strengths of the echoes and the Doppler spectra are prescribed (Figure 12).

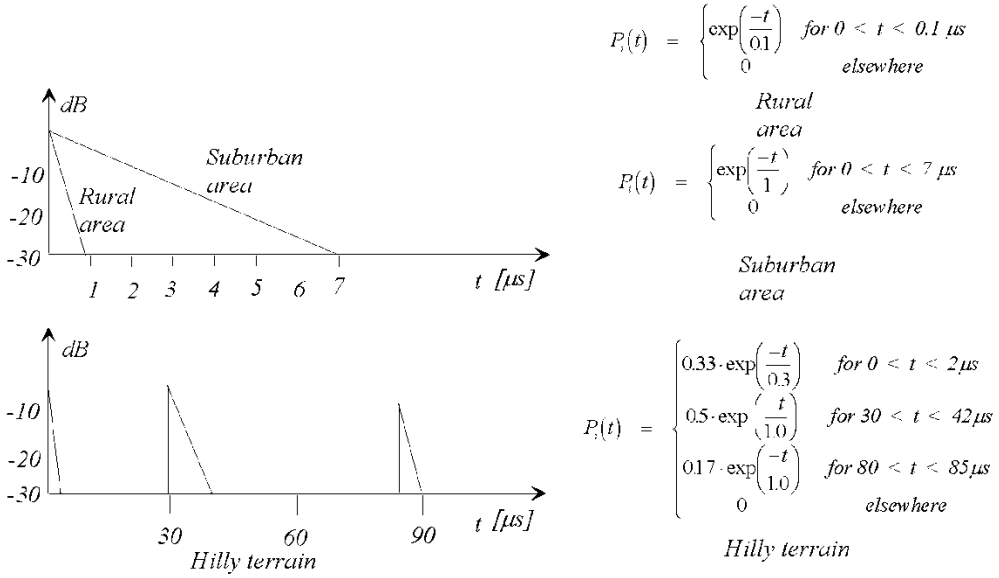


Figure 12: Typical landscape profiles [1]

Doppler Effect

Since the mobile receiver and some of the reflecting objects are in motion, the receive frequency is shifted because of the Doppler Effect. In the case of single-path reception this shift is calculated as follows:

$$f_d = \frac{v}{c} f_c \cos\alpha \tag{3}$$

where v = speed of vehicle

c = speed of light

f = carrier frequency

α = angle between v and the line connecting transmitter and receiver

In the case of multipath reception the signals on the individual paths arrive at the receiving antenna with different Doppler shifts because of the different angles α_i , and the receive spectrum is spread. Assuming an equal distribution of the angles of incidence, the power density spectrum can be calculated as follows:

$$P(f) = \frac{1}{\pi} \frac{1}{\sqrt{f_d^2 - f^2}} \text{ for } |f| < |f_d| \tag{4}$$

where f_d = maximum Doppler frequency.

where f = max. Doppler frequency

Of course, other Doppler spectra are possible in addition to the pure Doppler shift described above; for example, spectra with a Gaussian distribution using one or several maxima. A Doppler spread can be calculated from the Doppler spectrum analogously to the delay spread (Figure 13).[1]

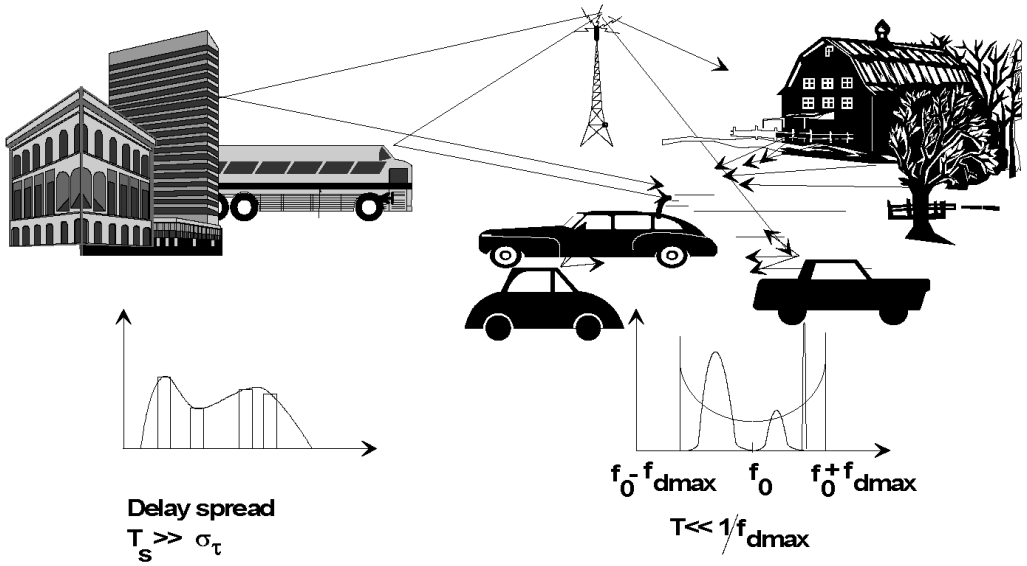


Figure 13: Doppler spread [1]

Some Examples:

Figure 14 shows a complex waveform which is needed for testing modern receivers, such as Software Defined Radios. Signal generators that can handle this are using a combination of many techniques. I will address this later.

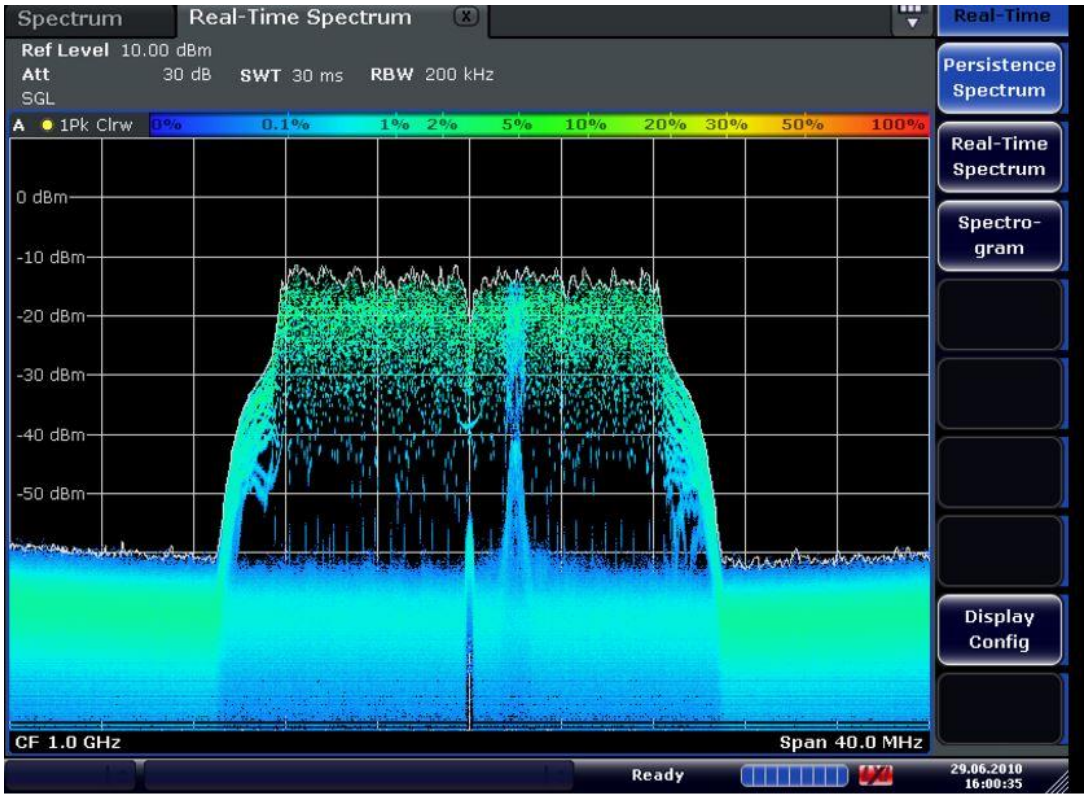


Figure 14: A Wi-Fi Wideband Signal Including a Discrete Carrier

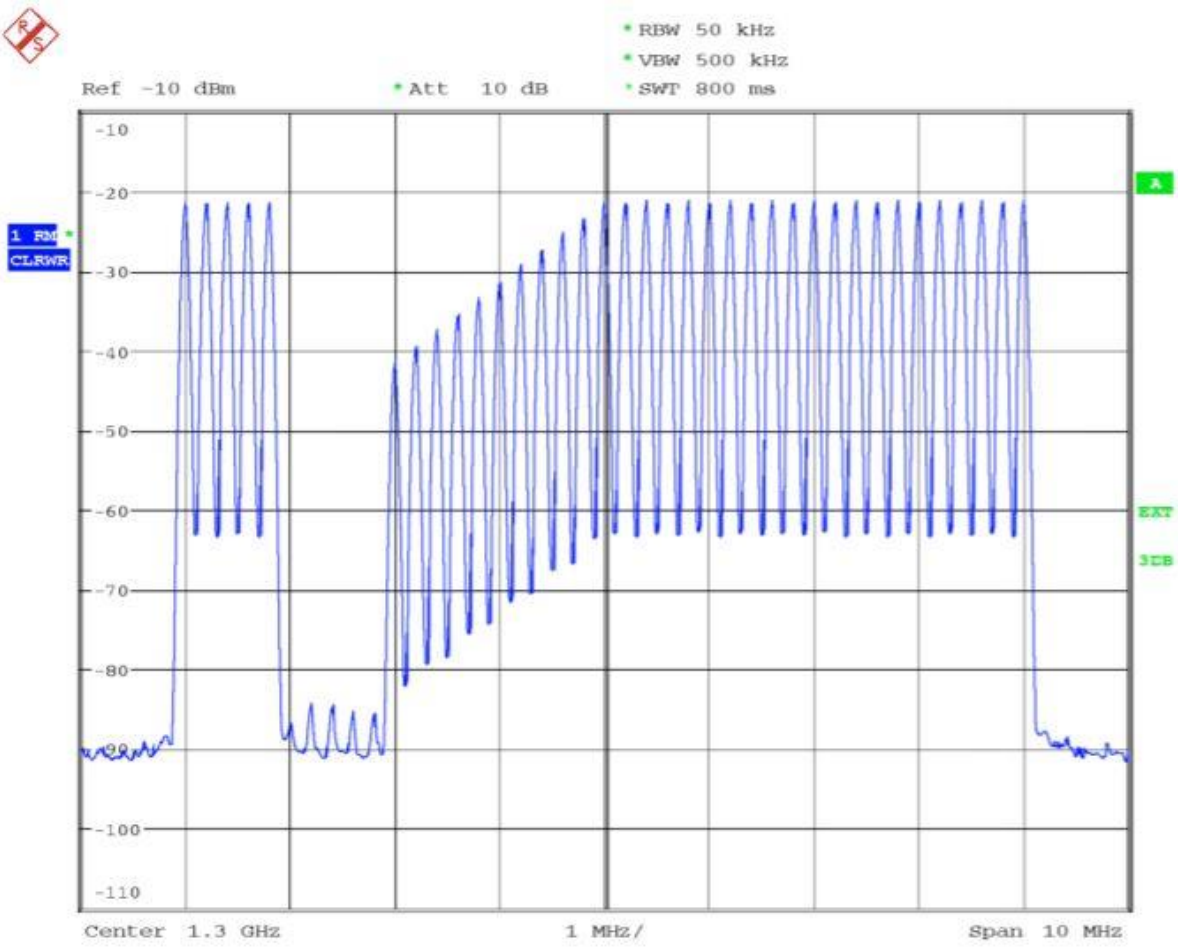


Figure 15: Example of multicarrier CW, with different carrier powers and some carriers switched off in the left half of the spectrum, I/Q level 0.5V (meas.). This is needed for advanced receiver testing

Why this presentation:

As seen above, the modern signal generator must be able to simulate these effects like fading, Doppler Effect, multi-pass signal, to really test the implemented system and algorithm (receiver).

Part I:

The Analog Signal Generator:

The next part will cover this, and then we will move to the digital signal generation in the part two. At the end we will look at hybrid combinations.

So now let us take a look at today's signals as we meet them when doing signal detection and analysis.

It is obvious that the generation of such a really wide band signal requires quite some modulation design techniques.

These modern generators are also used for performance testing of "Software Defined Radio's"

And it is not surprising that sometimes the internal numerically controlled oscillator, DDS based, close in phase noise, maybe better than the test generator.

The book Communications Receivers, see below, has a dedicated chapter about testing the performance of both analog and digital receivers.

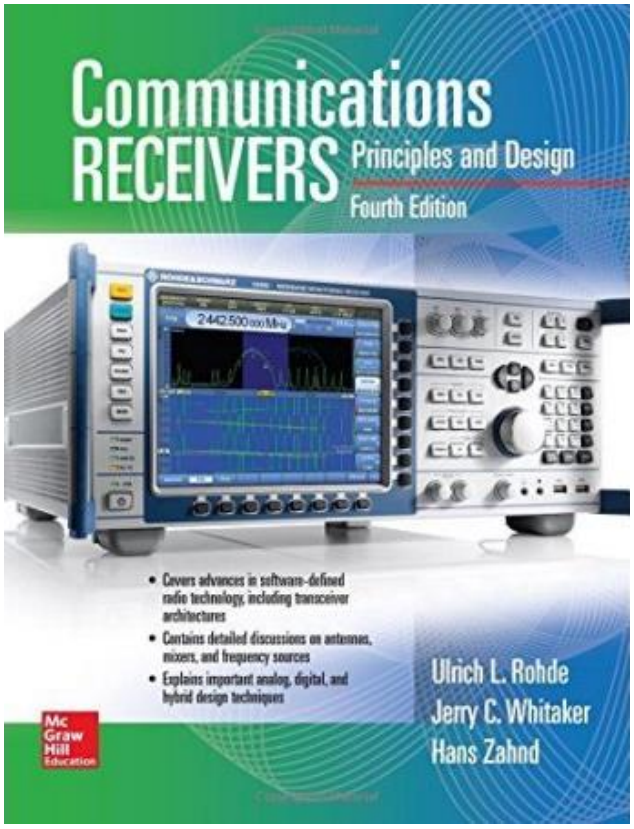


Figure 16: Communication Receivers – Principle and Design

While this book title (Figure 16) says receivers, a short part of it addresses the transmitter part.

Here is a block diagram of an analog transceiver and the earlier signal generators were designed to allow the measurements of the receiver part.

From analog radios to software defined radio

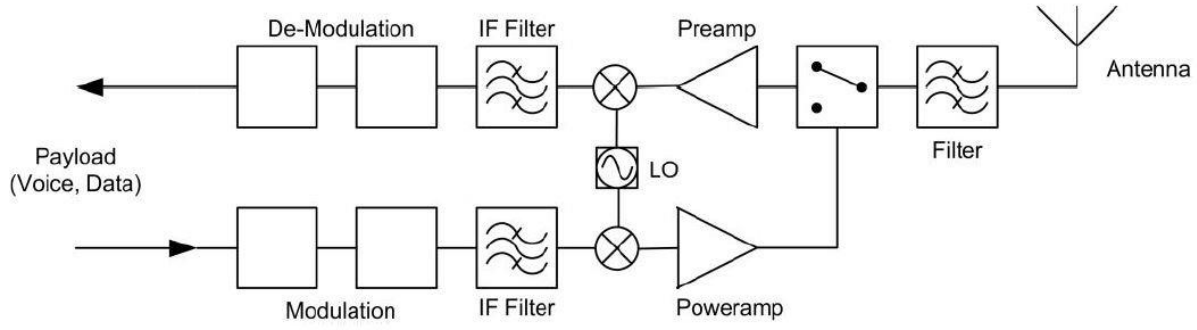


Figure 17: Conventional analog (hardware) radio (simplified)

Figure 17 provides a block diagram of a classic hardware radio, split into the receiver and the transmitter branches. The received signal is first filtered and preamplified. It is then downconverted from the carrier frequency to an intermediate frequency (this can take place over several steps). The signal is filtered once again and then demodulated. The (de)modulation block can be either analog or digital.

Also, here is a short list of parameters of interest to be determined for an analog radio. What's the difference? It's the determination of the large signal dynamic range, which will be different for SDRs.

Receiver tests
Receiver sensitivity and associated characteristics
Demodulation characteristics
Dynamic sensitivity and desensitization
Spurious response and IF rejection
Intermodulation response (out of band)
Blocking
Oscillator emission
Cross modulation rejection
Receiver response time

Over the past decades huge progress has been made in developing new types of oscillators and amplifiers and modulation applications, both amplitude and frequency related and a combination of both.

This 4 channel test is a real life requirement, which the traditional generators cannot handle. This can only be done with I/Q based advanced Vector Signal Generator using arbitrary wave generation.

The following is an example of how such a signal looks like.

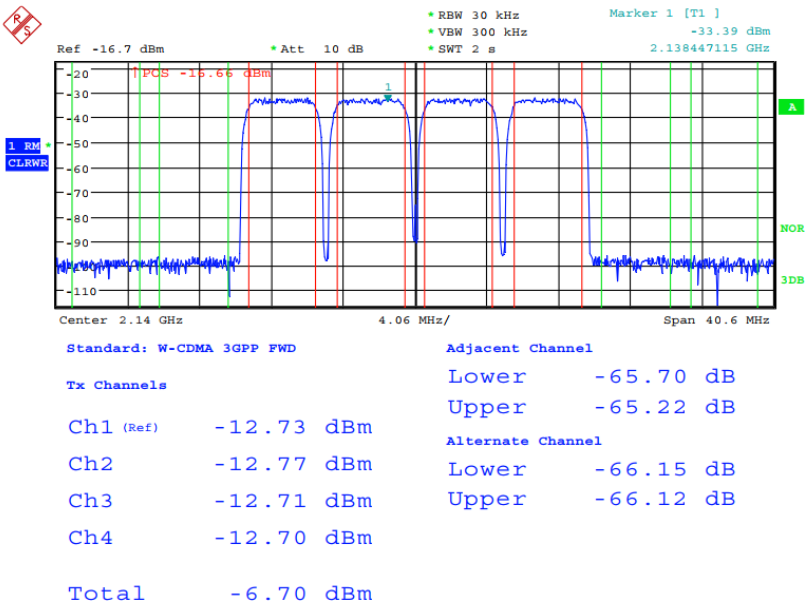


Figure 18: Measured ACPR for a 3GPP four-carrier signal with test model 1, 64 DPCH on each carrier (baseband gain: +3dB)

I will now show the development from simple analog based signal generators using different resonators, to synthesizers with still analog modulation capabilities, to "direct digital synthesizer with arbitrary waveform generators" to finally modern hybrid synthesizers that combine the best of both worlds. Also opto electrical applications will be considered

Signals need to be stable, pure (minimal spurious signals), clean (minimal phase noise) and of sufficient output power.

The following shows the measured phase noise of the best analog synthesizer currently on the market (2018)

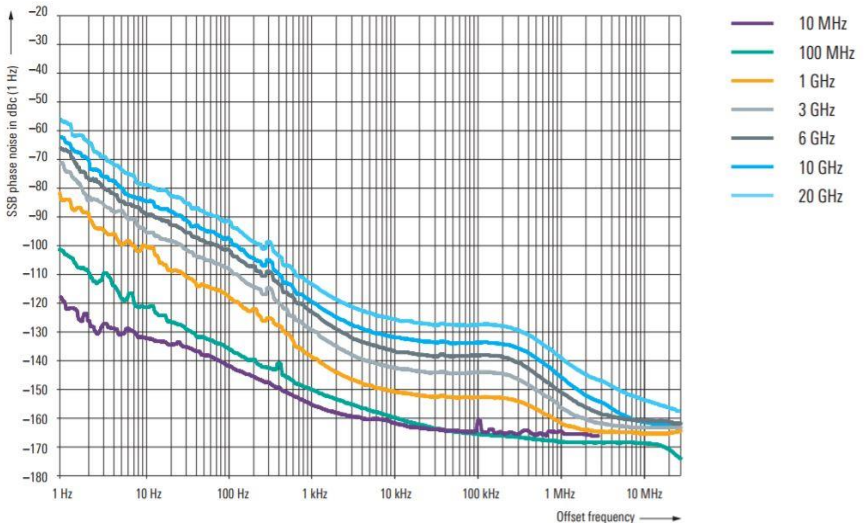


Figure 19: The measured phase noise of a modern clock synthesized generator

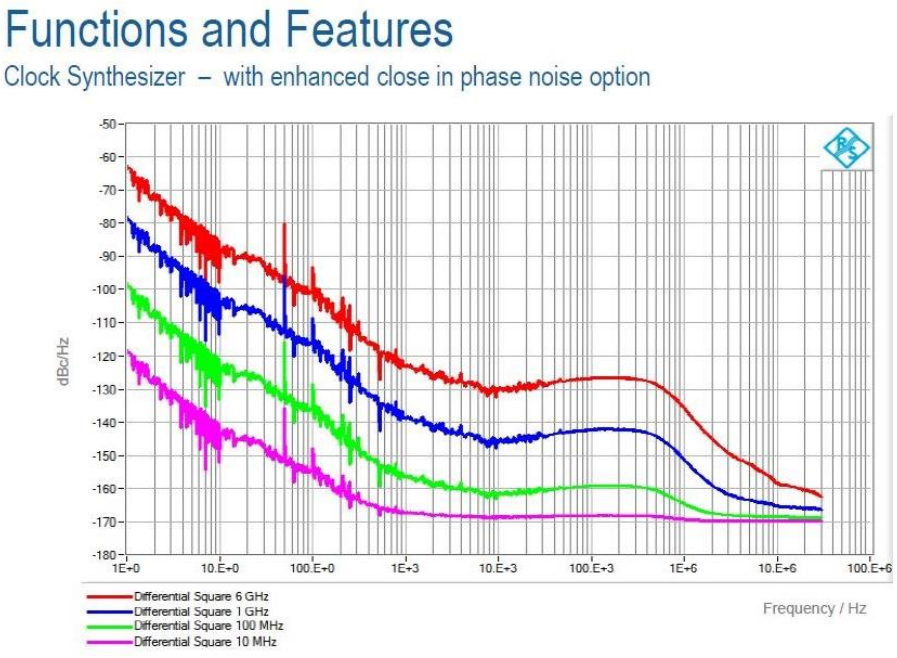


Figure 20: R&S SMA100 Functions and Features – Clock Synthesizer – with enhanced close-in phase noise option

Figure 21: R&S SMA 100B

These performance capabilities in an analog signal generator are found in the new R&S SMA 100B. This covers 8 kHz to above 20GHz, depending on the options.

In the “digital” signal generation section the tools and tricks will be described that are needed.

If all combined, is now the resulting signal generator a "Vector Signal Generator" useful for a host of applications, and covers the range upto 40GHz.

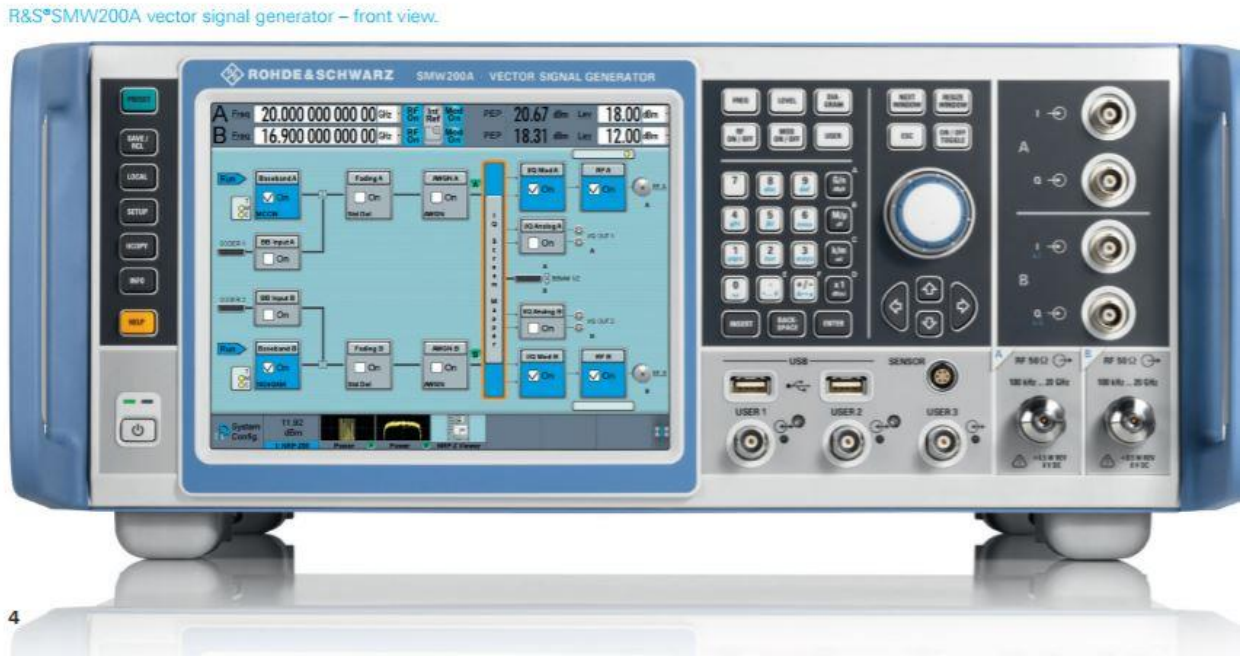


Figure 22: R&S Vector Signal Generator – SMW200A

More details about signal generation and synthesizers will be in my forthcoming book, Figure 23.

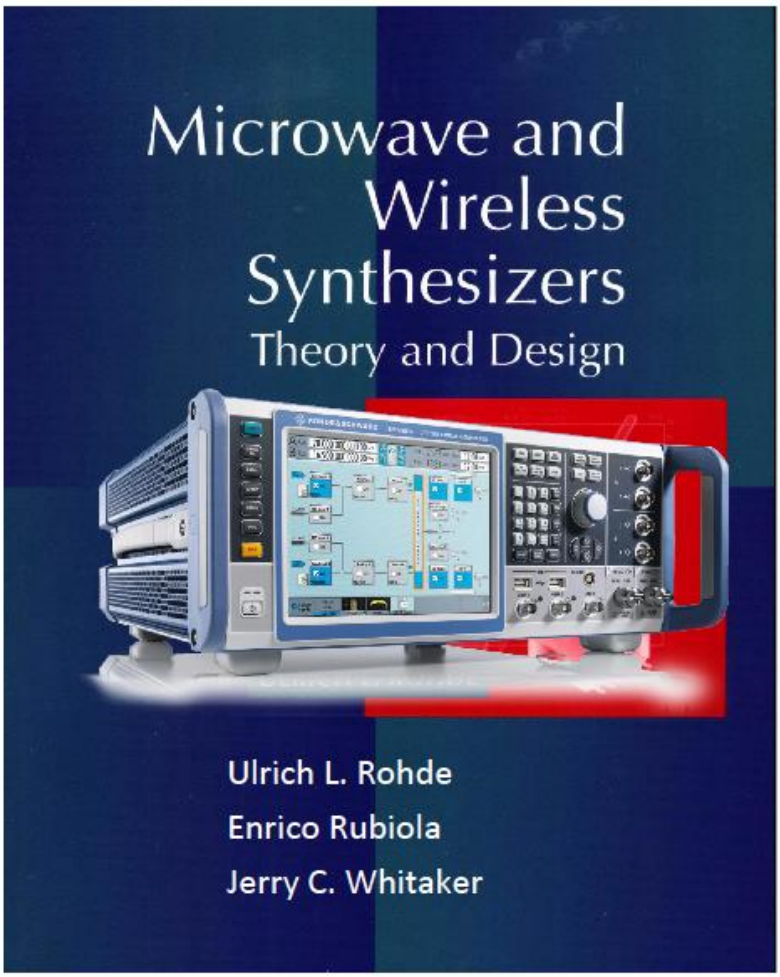


Figure 23: Microwave and Wireless Synthesizers –Theory and Design

Since the oscillator is the key part of any signal generator, besides having a power supply, AM and FM modulator, buffer/output amplifier, output filter is needed.

Now some technical details about oscillators:

The majority of LC based oscillators are based on the Colpitts oscillator design.

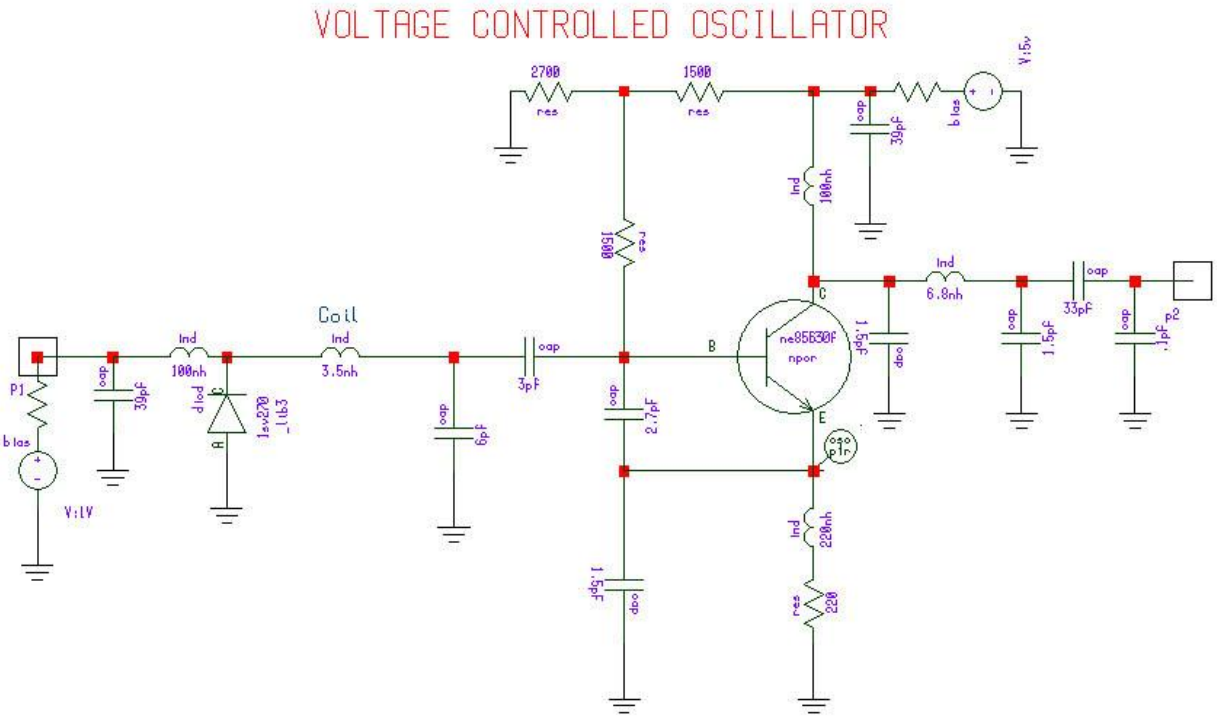


Figure 24: Schematic diagram form of the linear model of an oscillator [3]

Figure 24 is the schematic of a voltage-controlled Colpitts-type oscillator. The Colpitts circuit is recognized by the capacitive feedback network comprised of the capacitors connected between base and emitter and emitter to ground. For frequency tuning, a tuning diode, varactor diode, has been added.

Figure 25 shows, in block diagram form, the linear model of an oscillator. It contains an amplifier with frequency-dependent forward loop gain $G(j\omega)$ and a frequency-dependent feedback network $H(j\omega)$. This network is typically the resonator which will determine the oscillation frequency. Its figure of merit Q should be made as high as possible.

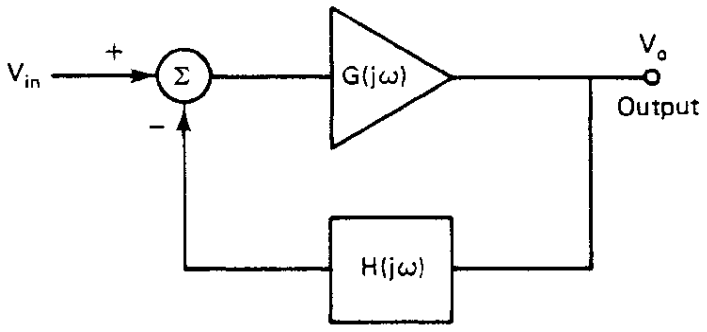


Figure 25: Block diagram of an oscillator showing forward and feedback loop components [3]

The output voltage is given by

$$V_o = \frac{V_{\text{in}} G(j\omega)}{1 + G(j\omega)H(j\omega)} \quad (5)$$

For an oscillator, the output V_o is nonzero even if the input signal V_{in} = 0. This can only be possible if the forward loop gain is infinite (which is not practical), or if the denominator

$$1 + G(j\omega)H(j\omega) = 0 \quad (6)$$

at some frequency ω_o. This leads to the well-known condition for oscillation (the *Nyquist criterion*), where at some frequency ω_o

$$G(j\omega_o)H(j\omega_o) = -1 \quad (7)$$

That is, the magnitude of the open-loop transfer function is equal to 1:

$$\left|G(j\omega_o)H(j\omega_o)\right| = 1 \quad (8)$$

and the phase shift is 180°:

$$\arg\left[G(j\omega_o)H(j\omega_o)\right] = 180° \quad (9)$$

This can be more simply expressed as follows: if in a negative-feedback system, the open-loop gain has a total phase shift of 180° at some frequency ω_o, the system will oscillate at that frequency provided that the open-loop gain is unity. If the gain is less than unity at the frequency where the phase shift is 180°, the system will be stable, whereas if the gain is greater than unity, the system will be unstable. [3]

This statement is not correct for some complicated systems, but it is correct for those transfer functions normally encountered in oscillator design. The conditions for stability are also known as the *Barkhausen criterion*, which states that if the closed-loop transfer function, is

$$\frac{V_o}{V_{in}} = \frac{\mu}{1 - \mu\beta} \quad (10)$$

where μ is the forward voltage gain and β is the feedback voltage gain, the system will oscillate provided that $\mu\beta$ = 1. This is equivalent to the Nyquist criterion, the difference being that the transfer function is written for a loop with positive feedback. Both versions state that the total phase shift around the loop must be 360° at the frequency of oscillation and the magnitude of the open-loop gain must be unity at that frequency.

The Colpitts oscillator in more detail

In the practical case, the device parasitics and loss resistance of the resonator will play an important role in the oscillator design. Figure 26 incorporates the base lead-inductance L_p and the package-capacitance C_p.

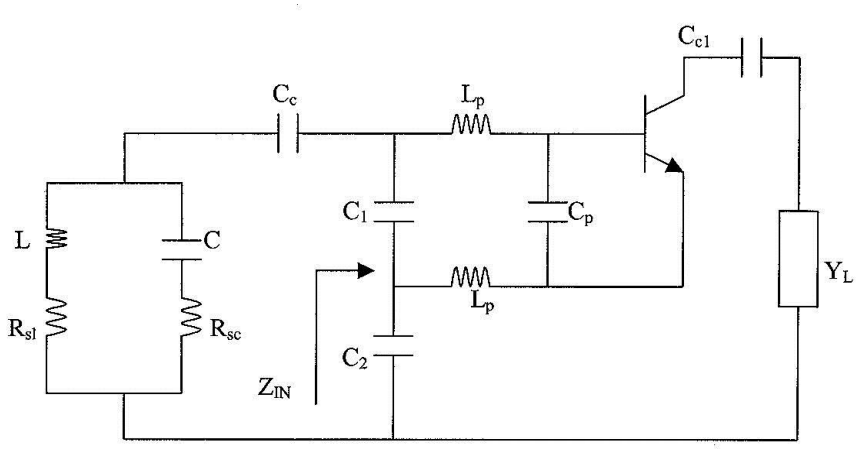


Figure 26: Colpitts oscillator with base-lead inductances and package capacitance, C_c is neglected [3]

The expression of input impedance is given as [15]

$$Z_{IN}\big|_{pacakage} = -\left[\frac{Y_{21}}{\omega^2(C_1+C_p)C_2}\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right] - j\left[\frac{(C_1+C_P+C_2)}{\omega(C_1+C_P)C_2} - \frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\frac{Y_{21}}{\omega(C_1+C_P)C_2}\right]$$

The real part is negative in value and compensates the losses of the tuned circuit, the oscillation will get started. [3][15]

This is the linear approach.

The resulting phase noise can be described by the equation combination of Leeson, Scherer and Rohde contributions as follows [3]:

$$£(f_m) = 10\log\left\{\left[1+\frac{f_0^{\,2}}{(2f_mQ_L)^2(1-\frac{Q_L}{Q_0})^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_o}+\frac{2kTRK_0^2}{f_m^{\,2}}\right\} \quad (11)$$

where £(f_m), f_m, f_0, f_c,Q_L,Q_0, F, k, T, P_0, R, and K_0 is the ratio of the sideband power in a 1Hz bandwidth at f_m to total power in dB, offset frequency from the carrier, carrier frequency, flicker corner frequency, loaded Q of the tuned circuit, unloaded Q of the tuned circuit, noise factor, Boltzmann's constant, temperature in degree Kelvin, average power at oscillator output, equivalent noise resistance of tuning diode, and oscillator voltage gain.

When adding an isolating amplifier the noise of an *LC* oscillator is determined by

$$£(f_m) = 0.5\times 10log\left[\left(S_\emptyset(f_m)\right)\right] = 0.5\times 10log\left\{\frac{\left[a_RF_0^4+a_E\left(\frac{F_0}{(2Q_L)}\right)^2\right]}{f_m^3}+\left[\frac{\left(\frac{2GFkT}{P_0}\left(\frac{F_0}{(2Q_L)}\right)^2\right)}{f_m^2}\right]+\left(\frac{2a_RQ_LF_0^3}{f_m^2}\right)+\frac{a_E}{f_m}+\frac{2GFkT}{P_0}\right\} \quad (12)$$

Where,

G = compressed power gain of the loop amplifier

F = noise factor of the loop amplifier

k = Boltzmann's constant

T = temperature in kelvins

P_0 = carrier power level (in watts) at the output of the loop amplifier

F_0 = carrier frequency in Hz

f_m = carrier offset frequency in Hz

$Q_L(=\pi F_0\tau_g)$ = loaded *Q* of the resonator in the feedback loop

a_R *and* a_E = flicker noise constants for the resonator and loop amplifier, respectively.

The problem with this design equation, everyone likes to quote, that it works after the fact. That means the designer does not know the output power, the flicker corner frequency, and the large signal noise figure, and finally as the right part of the equation is the noise from the tuning diode, the value of the equivalent noise resistor R!

If the energy is taken carefully from the resonator the far off phase noise can be as low as -175dBc/Hz below the carrier.

It needs to be noted that the phase noise is proportional to $1/Q_L^2$

There are two additional topics to be considered. The voltage-controlled oscillator (VCO) is used rarely stand alone, but mostly in a PLL system, and followed by a buffer / isolation stage [1]

Unfortunately the ultimate phase noise is determined by the buffer/isolation amplifier.

Most of the resonators in an oscillator can be expressed by an LC equivalent. See the Collpits Oscillator above. Additional typical resonators are crystals, SAW resonators, dielectric resonators, even YIG resonators.

The use of transmission lines instead of LC circuits can improve the noise performance, as shown below.

In order to compare the oscillators with lumped and distributed parameters for the purpose of the best phase noise characteristics, it is sufficient to determine the susceptance sensitivity S_0 for each oscillator circuit with equal capacitances. For a simple parallel lumped resonant circuit shown in Figure 27,

$$S_0 = \frac{\partial}{\partial\omega}\left(\omega C - \frac{1}{\omega L}\right) = C\left(1 + \frac{1}{\omega^2 LC}\right)\Big|_{\omega=\omega_0} \tag{13}$$

The oscillator parallel resonant circuit with uniform transmission line is shown in Figure 27b. Since the ratio between the transmission line electrical length θ and the frequency

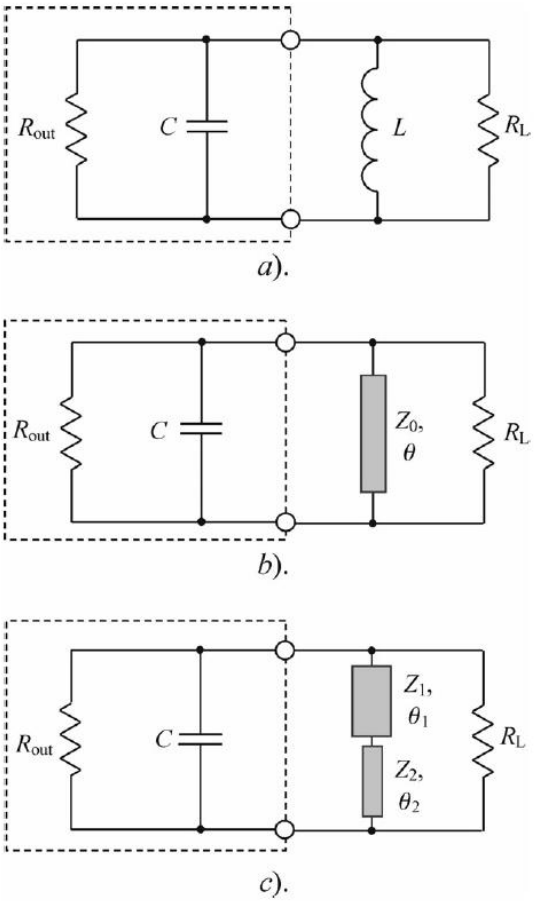


Figure 27: Equivalent parallel oscillator resonant circuits with (a) lumped parameters and (b, c) distributed parameters [2]

ω is defined as

$$\theta = \omega l \sqrt{\varepsilon_r}/c \tag{14}$$

where l is the length of the transmission line, ε_r is the dielectric permittivity, c is the free-space velocity of light, the following condition is met:

$$\frac{\partial \theta}{\partial \omega} = \frac{\theta}{\omega} \tag{15}$$

Then, by taking into account that $C = 1/\omega_0 Z_0 \tan\theta$ at resonant frequency, the sensitivity S_0 for the parallel resonant circuit with a lossless uniform transmission line is obtained as

$$S_0 = \frac{\partial}{\partial \omega}\left(\omega C - \frac{1}{Z_0 \tan\theta}\right) = C\left(1 + \frac{\theta}{\omega C Z_0 \sin^2\theta}\right)\Bigg|_{\omega=\omega_0} = C\left(1 + \frac{2\theta}{\sin 2\theta}\right) \tag{16}$$

Similarly, the susceptance sensitivity S_0 for the parallel resonant circuit with lossless two-section transmission line of equal section lengths $\theta_1 = \theta_2 = \theta/2$ shown in Figure 27(c) can be written as

$$S_0 = \frac{\partial}{\partial \omega}\left(\omega C - \frac{1}{Z_1 \tan\frac{\theta}{2}} \frac{1 - M\tan^2\frac{\theta}{2}}{1+M}\right)\Bigg|_{\omega=\omega_0} = C\left(1 + \frac{\theta}{\sin\theta}\frac{1 + M\tan^2\frac{\theta}{2}}{1 - M\tan^2\frac{\theta}{2}}\right) \tag{17}$$

Figure 28 shows the frequency dependencies of the normalized sensitivity S_0/C for different types of oscillator circuits. For a lumped resonant circuit, $S_0/C = 2$, which means that it is independent of frequency. For the resonant circuits with transmission lines, the value of the sensitivity S_0 for a given capacitance C can be increased significantly by an appropriate increase of θ. If $\theta = 40°$, $S_0/C = 2.42$ for the resonant circuit with uniform transmission line, [2]

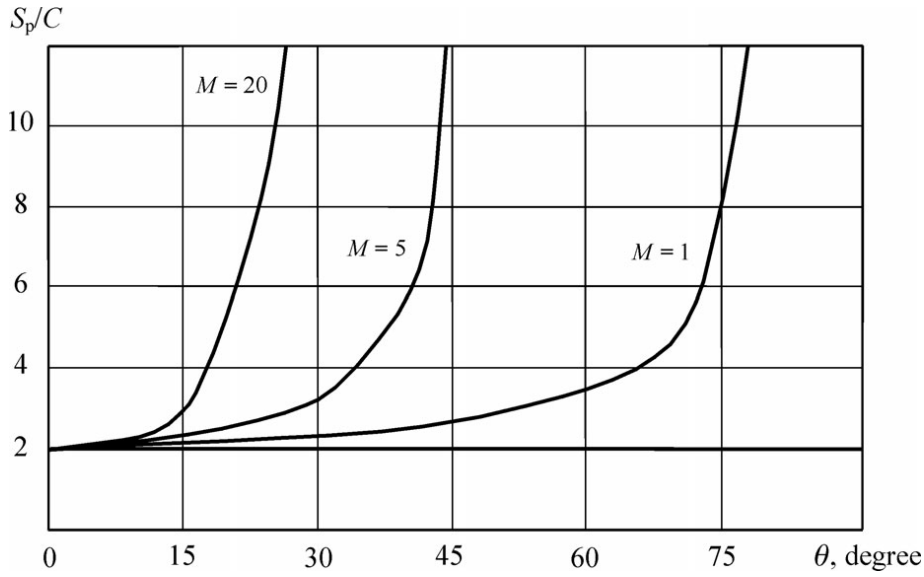


Figure 28: Frequency dependencies of the normalized susceptance sensitivity S_0/C for different characteristic impedance ratio M [2]

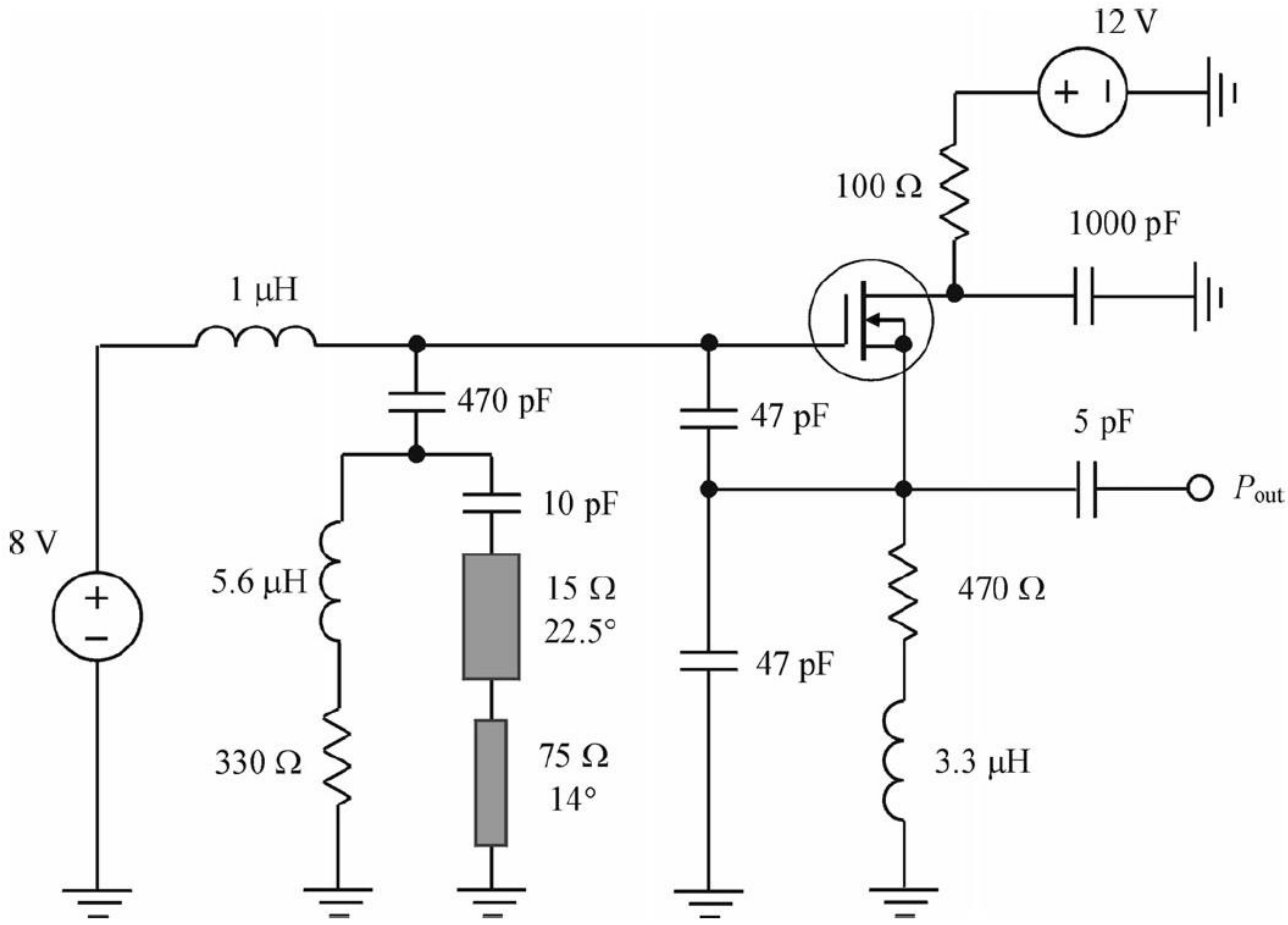


Figure 29: Equivalent circuit of the MOSFET oscillator with two-section line [2]

Whereas the use of the two-section transmission line with M=5 results in S_0/C=6.3.5. In the case of θ=24°, by using of the two-section transmission line with M=20, it is possible to increase the value of S_0/C by a factor of more than ten. For the same values of S_0/C, the use of the two-section transmission line with a high value of M enables one to reduce the total electrical length of the transmission line by a factor of three to four.

As evidence of how moving from lumped to distributed techniques can improve oscillator performance at frequencies where *LC* tanks become problematic, the next figure compares, for a simulated BJT Colpitts oscillator operating at 2.3 GHz, the difference in phase-noise performance obtainable with a resonator consisting of an ideal 2-nH inductor and a 1/4-λ transmission-line (11Ω, 90° long at 2.6 GHz, attenuation 0.1 dB/meter) with the transistor biased by constant-current and constant-voltage sources.

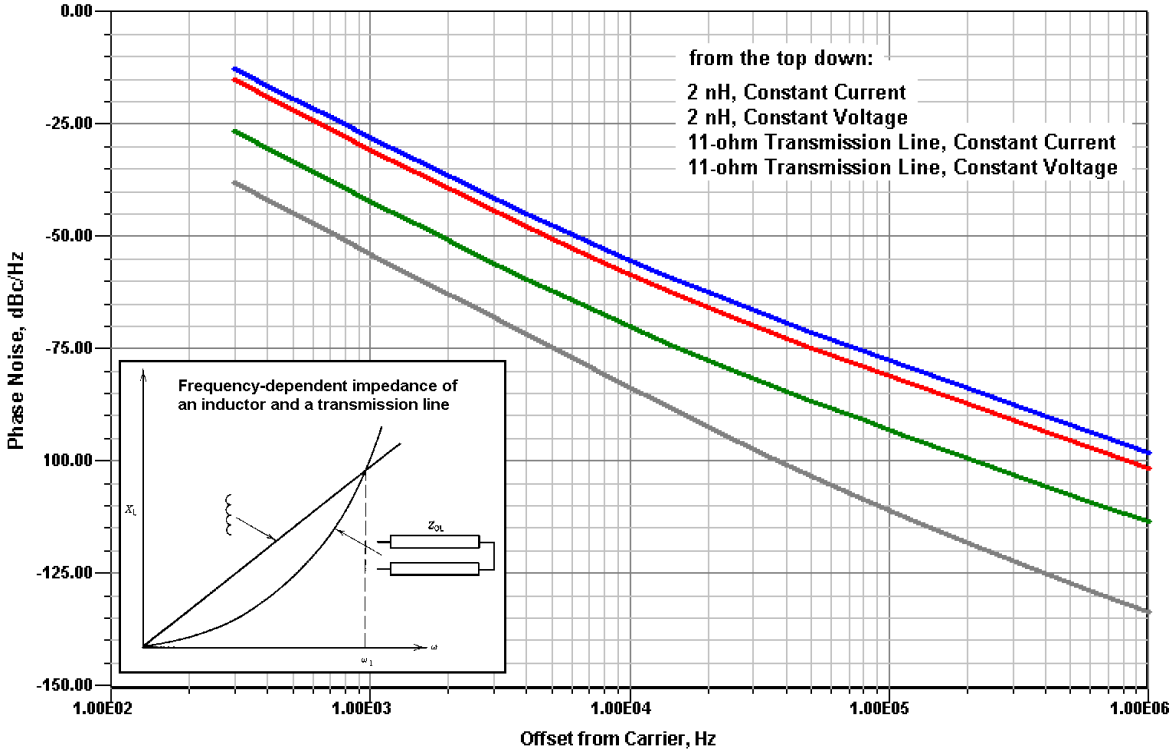


Figure 30: Shows the phase-noise performance of a 2.3-GHz BJT oscillator with a resonator consisting of an inductor (2nH) and a 1/4-λ transmission line (11Ω, approximating the behavior of a dielectric resonator) with bias from a constant-current source and a low-impedance, resistive constant-voltage source [1]

From the condition

$$\omega L = 1/\omega C$$

The Johnson resonant formula can be derived from this

$$f = 1/2\pi\sqrt{LC}$$

For the transmission line a hyperbolic $tanh$ function is added.

Here the length of the resonator and the material Epsilon constant play a role.

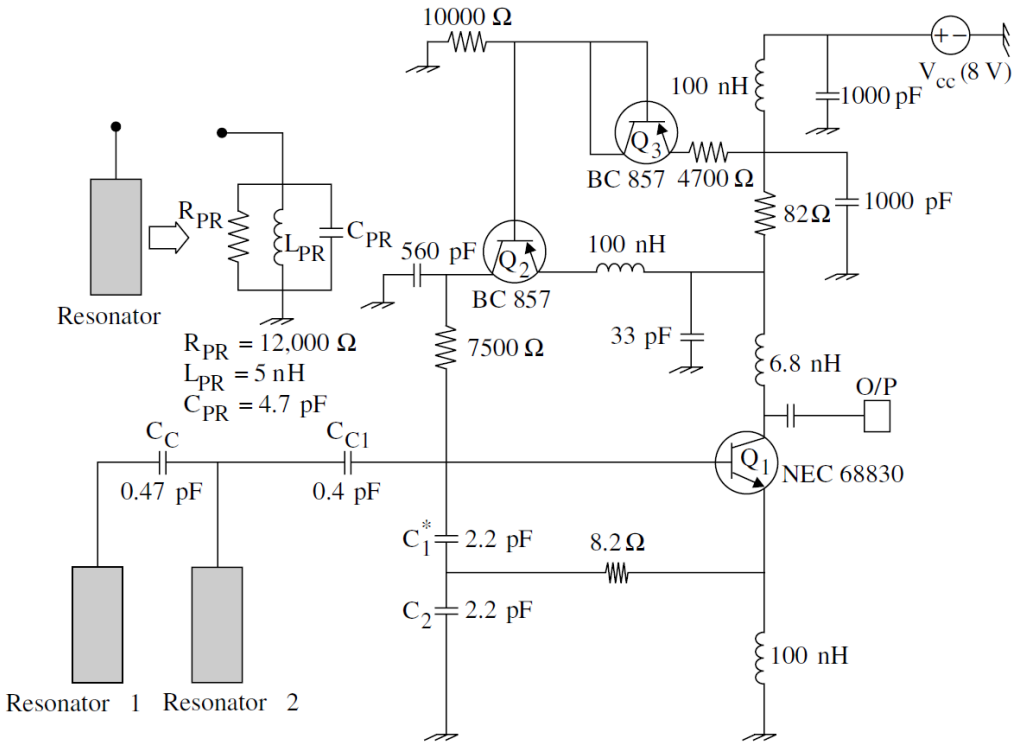


Figure 31: Two-Resonator Colpitts Oscillator Circuit [3]

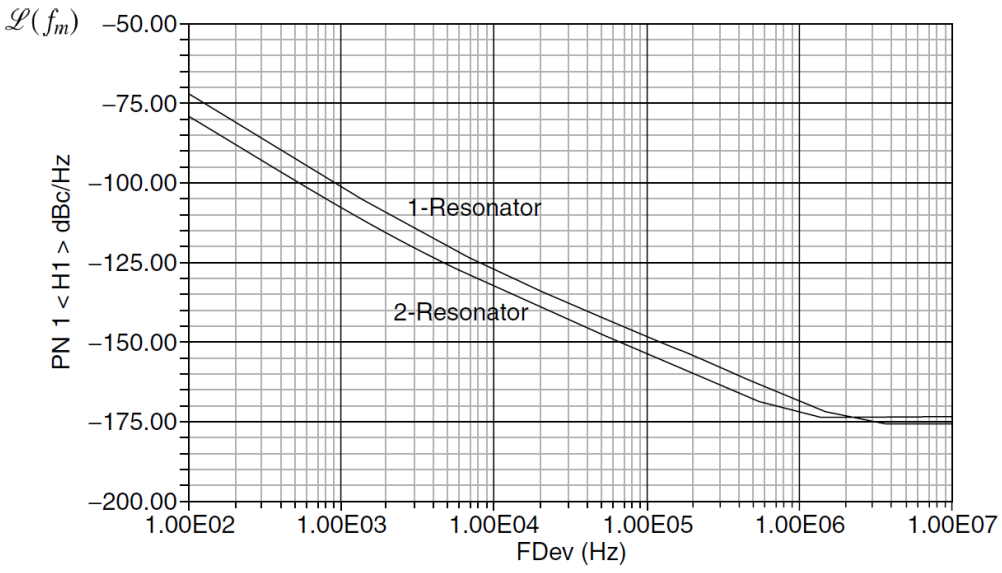


Figure 32: Simulated phase noise plot for the single resonator (1-resonator) and the coupled resonator (2-resonator) – The Phase Noise improves ~10dB with the use of a second resonator [3]

The tuning voltage (port) is typically connected to a PLL loop. Some versions use a coarse steering DC input and a modulation voltage input. For FM modulation of an auxiliary oscillator the PLL loop

bandwidth has to be less than the lowest modulation frequency. This older approach is now obsolete bus referred here for reason of completeness.

There is a practical limit how high in frequency an LC or equivalent oscillator should be design.

As the mechanical parts get lossy and the tuning diodes approach their cut off frequency, it is better to stay at a lower frequency, and double the frequency. The push-push oscillator solves this very well.

In the push-push circuit the fundamental frequency is ideally canceled and the first harmonic is available with better phase noise that a design at this frequency. See the circuit below:

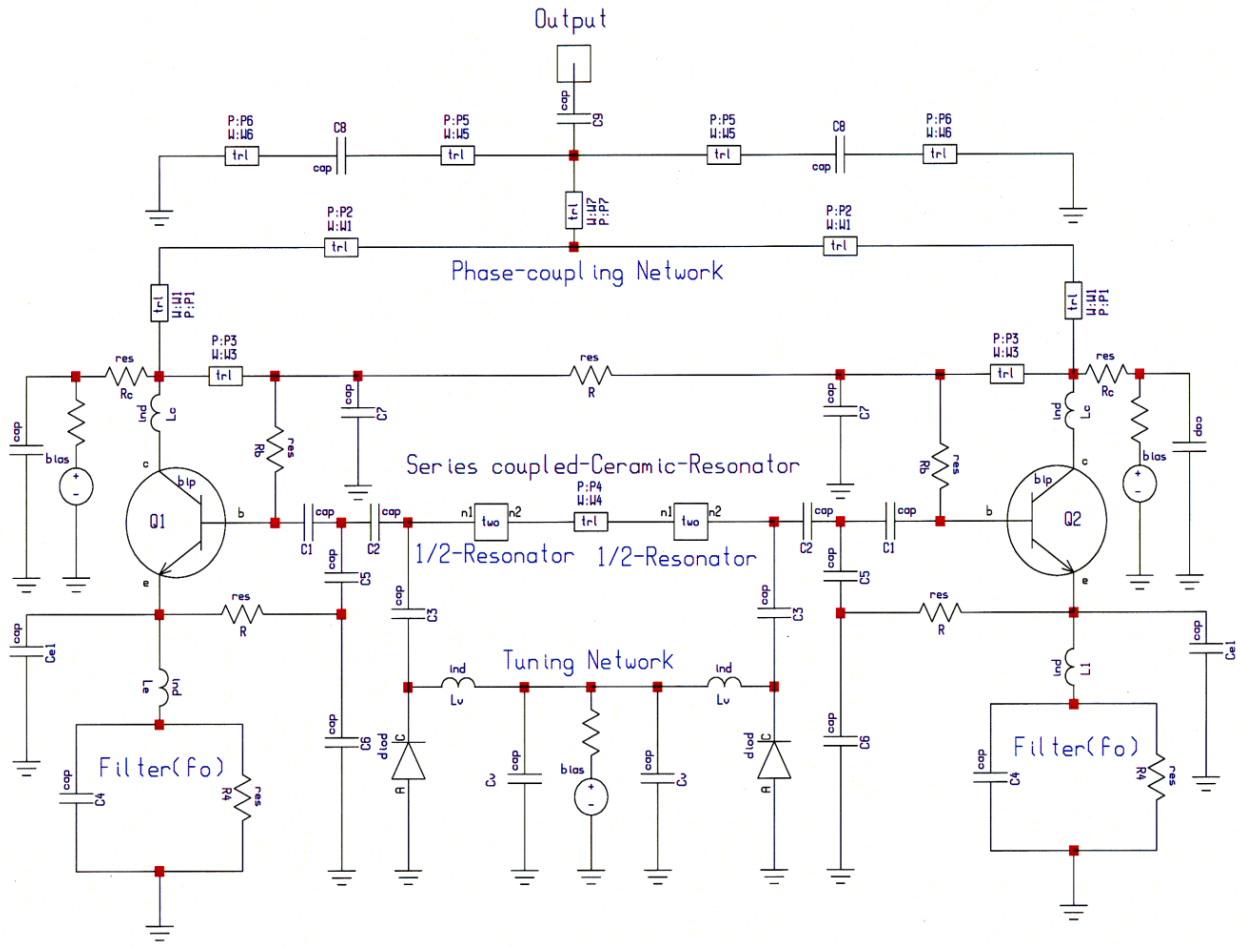
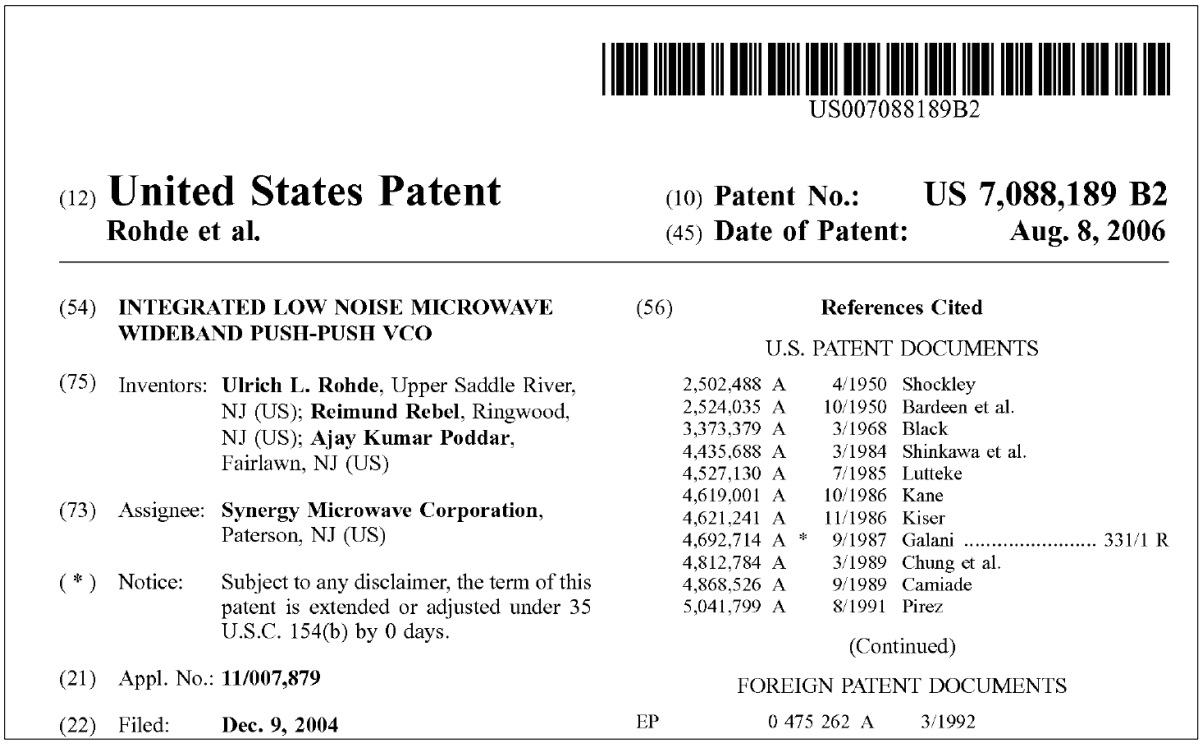


Figure 33: Push-Push Oscillator Circuit (see patent below) [4]



US007088189B2

(12) **United States Patent**
Rohde et al.

(10) **Patent No.: US 7,088,189 B2**
(45) **Date of Patent: Aug. 8, 2006**

(54) **INTEGRATED LOW NOISE MICROWAVE WIDEBAND PUSH-PUSH VCO**

(75) Inventors: **Ulrich L. Rohde**, Upper Saddle River, NJ (US); **Reimund Rebel**, Ringwood, NJ (US); **Ajay Kumar Poddar**, Fairlawn, NJ (US)

(73) Assignee: **Synergy Microwave Corporation**, Paterson, NJ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/007,879**

(22) Filed: **Dec. 9, 2004**

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Figure 34: Patent for Push-push oscillator [4]

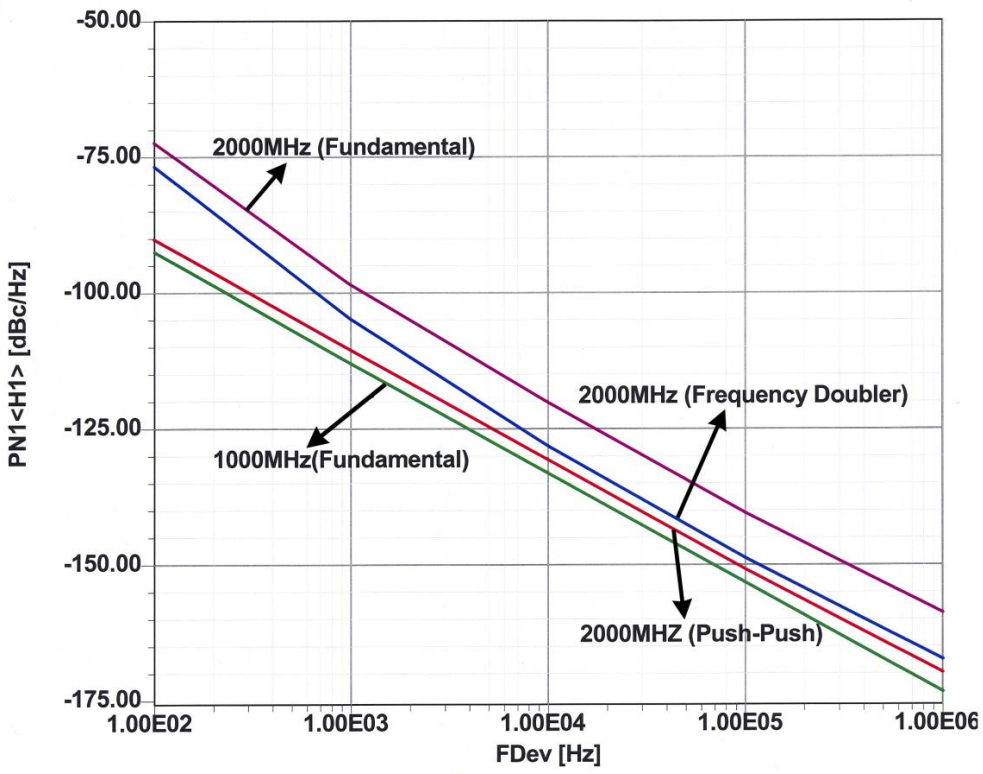


Figure 35: Demonstration of the Influence of the Tuning diode

The influence of the tuning diode [7]:

In order to calculate the contribution of the tuning diode, it is necessary to define an equivalent noise R_{aeq} that, inserted in Nyquist's equation,

$$V_n = \sqrt{4kT_o R\Delta f} \tag{18}$$

Where, kT_o = 4.2×10^{-21} at about 300K, R is the equivalent noise resistor, and Δf is the bandwidth, determines an open-circuit noise voltage across the tuning diode. Practical values of R_{aeq} for carefully selected tuning diodes are in the vicinity of 200 Ω to 50 kΩ. If we now determine the noise voltage $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 10{,}000}$, the resulting voltage value is 1.296×10^{-8} V$\sqrt{\text{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain K_o, resulting in the RMS frequency deviation

$$(\Delta f_{\text{rms}}) = K_o \times (1.296 \times 10^{-8}\ \text{V})\ \text{in 1 - Hz bandwidth} \tag{19}$$

To translate this into an equivalent peak phase deviation,

$$\theta_d = \frac{K_o\sqrt{2}}{f_m}(1.296 \times 10^{-8})\ \text{rad in 1 - Hz bandwidth} \tag{20}$$

Or, for a typical oscillator gain of 100 kHz/V,

$$\theta_d = \frac{0.00183}{f_m}\ \text{rad in 1 - Hz bandwidth} \tag{21}$$

For f_m = 2.4 kHz (typical spacing for adjacent-channel measurements for good SSB RF radios), then θ_c = 732 × 10^{-9}. This can be converted now into the SSB signal-to-noise ratio:

$$\mathcal{L}(f_m) = 20log_{10}\frac{\theta_c}{2} = -128dBc/Hz \tag{22}$$

The tuning diode adds significant noise, so if the above mentioned 1 KHz bandwidth for the PLL is used, at 2.4 KHz the oscillator dominates.

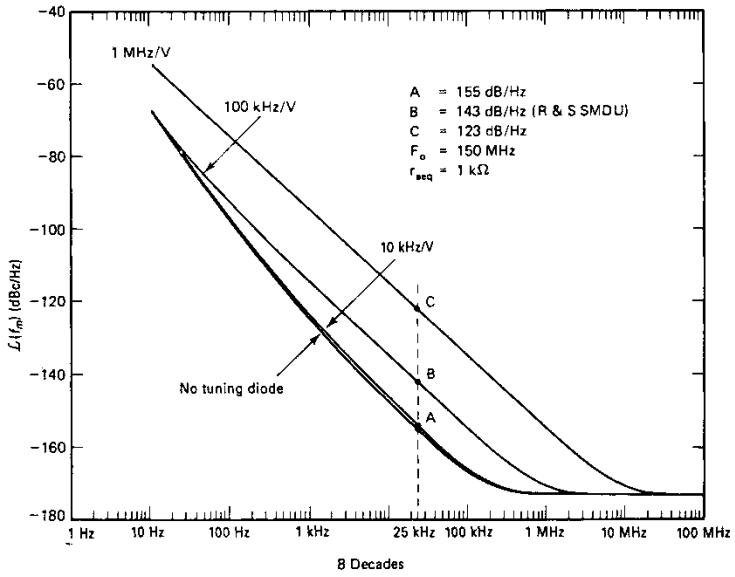


Figure 36: Shows the influence of the diode noise of a VCO at 150 MHz [7]

In case of B and C the tuning diode greatly ruins the overall phase noise regardless of a high loaded Q! The flicker frequency component also has a huge influence on the phase noise.

Figure 37 - shows the noise contribution of the flicker noise in a circuit with fixed Q.

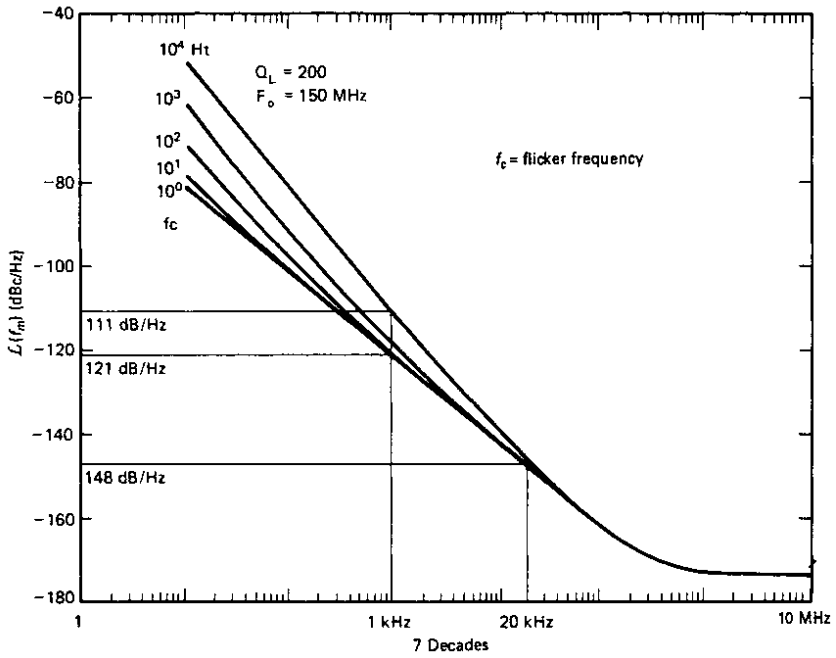


Figure 37: Shows the phase noise contribution of the flicker noise to the oscillator noise [7]

At 1 KHz offset the phase noise deteriates by 10 dB.

As mentioned earlier, these voltage controlled oscillators will become part of a PLL synthesizer.

A modern phase noise set of eqution for an oscillator:

Calculating the phase noise from circuit parameters and using large singal paramerters or derive these with the help from Besselfuntions, specifically obtaining Y21 large signal.

The total effect of all the four noise sources can be expressed as [3]

$$\pounds(\omega) = 10\log\frac{4KT}{\omega L \times Q}\left\{\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{\mathrm{Re}sonator} + 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{base-resis\tan ce}\right.$$
$$+\left[2qI_b + \frac{2\pi K_f I_b^{AF}}{\omega}\right]\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{2Q\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{flic\,\mathrm{ker}-base-current} \qquad (23)$$
$$\left.+2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\omega}\right]\right\}^2_{collector-current}\right]$$

A 144 MHz Oscillator Example: [8]

(Using Time Domain Parameters @ 1c=10mA

From the resonator R_P = 7056 Ohm (ωL x Q)

Q of the resonator = 200 (Q of the inductor at 144 MHz)

Resonator inductance = 39nH

Resonator capacitance = 22 pF

Collector current of the transistor I_c = 10 mA

Base current of the transistor I_b = 85uA.

Flicker noise exponent AF = 2

Flicker noise constant K_f = 1E-12

Feedback factor n = 5.

Phase noise @ 10 KHz:

$$PN_{(ibn+ifn)_i}(\omega_0 + 10KHz) \approx -134.2dBc/Hz$$

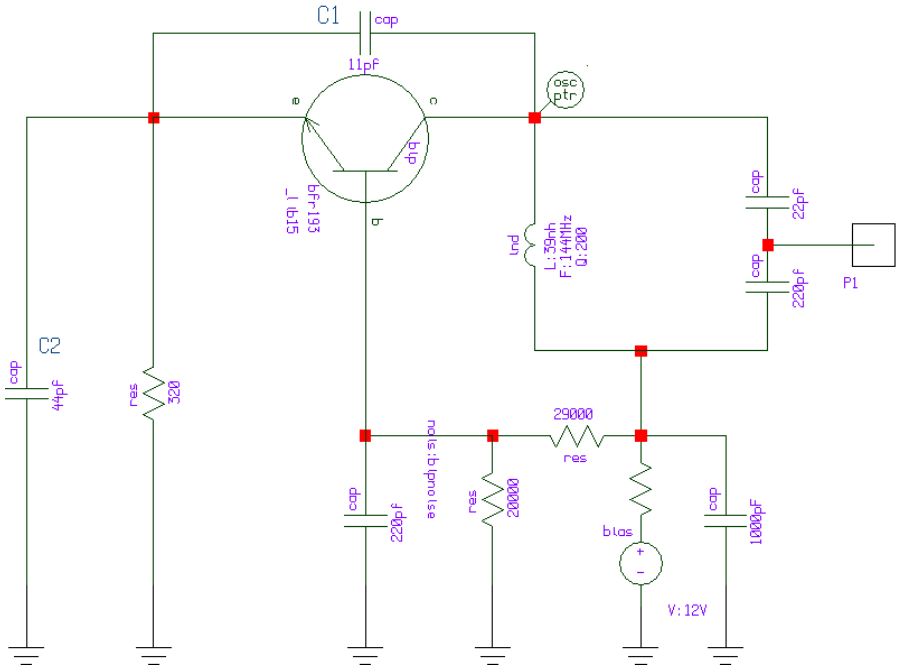
$$PN_{Vbn}(\omega_0 + 10KHz) \approx -151dBc/Hz$$

$$PN_{nr}(\omega_0 + 10KHz) \approx -169.6dBc/Hz$$

$$PN_{icn}(\omega_0 + 10KHz) \approx -150.6dBc/Hz$$

$$P_{out} = 5dBm$$

The 144 MHz Oscillator (Now using Time Domain Parameters @ 1c=10mA)



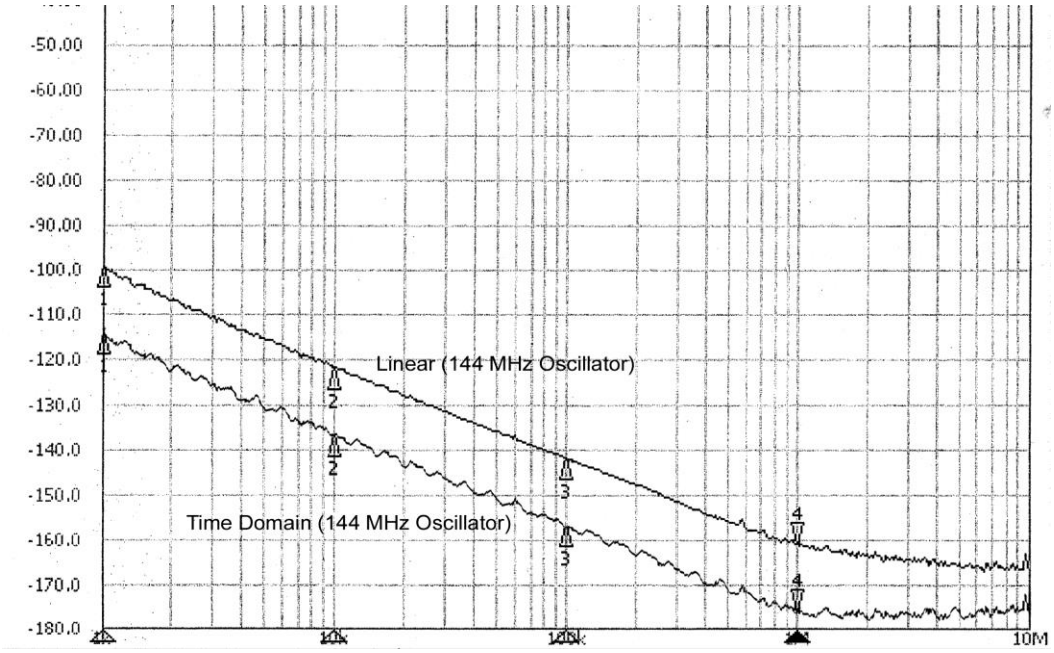


Figure 38: Meassured phase noise (Aeroflex) of the 144 MHz Oscillator design based on state of the art linear design, and based on optimised design using large signal parameters [8]

The value for KF=1e-12 is vaild for small currents, and in the equation above the main phase noise (measured) contribution is the resonator loss. For higher frequencies and higher output power (higher DC current, the flicker and DC current contribuion to the flicker noise will dominate. At 30 mA and higher a typcal KF factor of 1e-7 is common.

Going back to the large signal phase noise analysis , the following equation is realy the most modern result [3]:

$$\pounds(\omega) = 10 \times \log\left[\left[k_0 + \left(\frac{k^3 k_1 \left[\frac{Y_{21}^+}{Y_{11}^+}\right]^2 [y]^{2p}}{\left[Y_{21}^+\right]^3 [y]^{3q}} \right)\left(\frac{1}{(y^2+k)}\right)\right]\left[\frac{[1+y]^2}{y^2}\right]\right] \qquad (24)$$

where

$$k_0 = \frac{kTR}{\omega^2\,\omega_0^2 L^2 C_2^2 V_{cc}^2}$$

$$k_1 = \frac{qI_c g_m^2 + \frac{K_f I_b^{AF}}{4\omega} g_m^2}{\omega^2\,\omega_0^4 L^2 V_{cc}^2}$$

$$k_2 = \omega_0^4 (\beta^+)^2$$

$$k_3 = \omega_0^2 g_m^2$$

$$k = \frac{k_3}{k_2^2 C_2^2}$$

Where k_1, k_2, and k_3, are constant only for a particular drive level, with $y = \frac{C_1}{C_2}$. Making k_2 and k_3 also dependent on y, as the drive level changes.

It is now of interest to look at the 1965 R&S SMDU Helix resonator based oscillator. Here is its schematic for 60MHz.

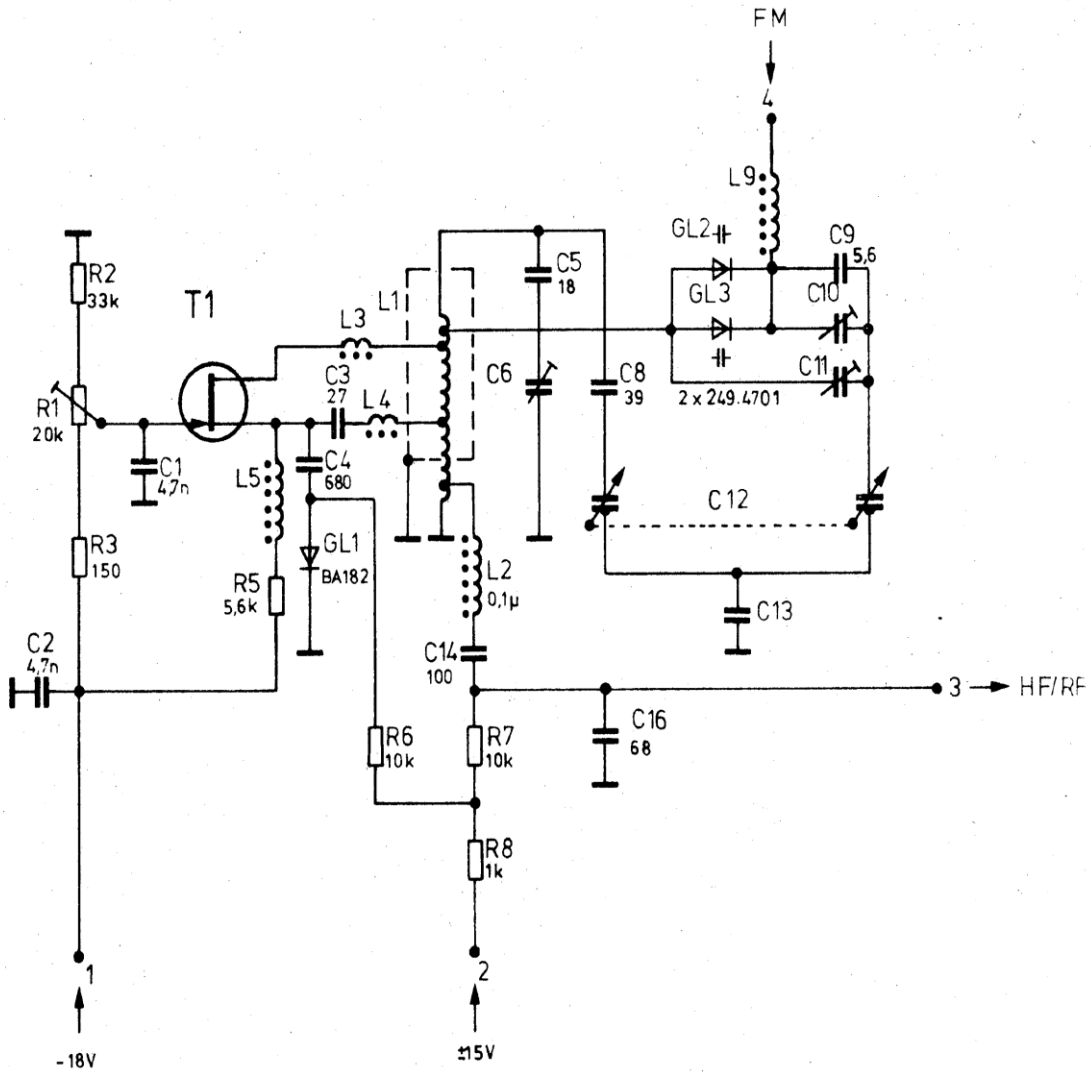


Figure 39: 60MHz Helix Resonator based Oscillator [R&S SMDU Service Manual]

It uses the 2N4416 FET and +/- 15 V source switches the oscillator on/off.

L1 is the helical resonator and C12 is the air variable capacitor.

L3, L4 and L5 are small RF chokes to avoid parasitic oscillations.

The noise improvement comes from the constant current source (5.6kΩ) in the source; the higher voltage drop is compensated by the positive voltage at the gate.

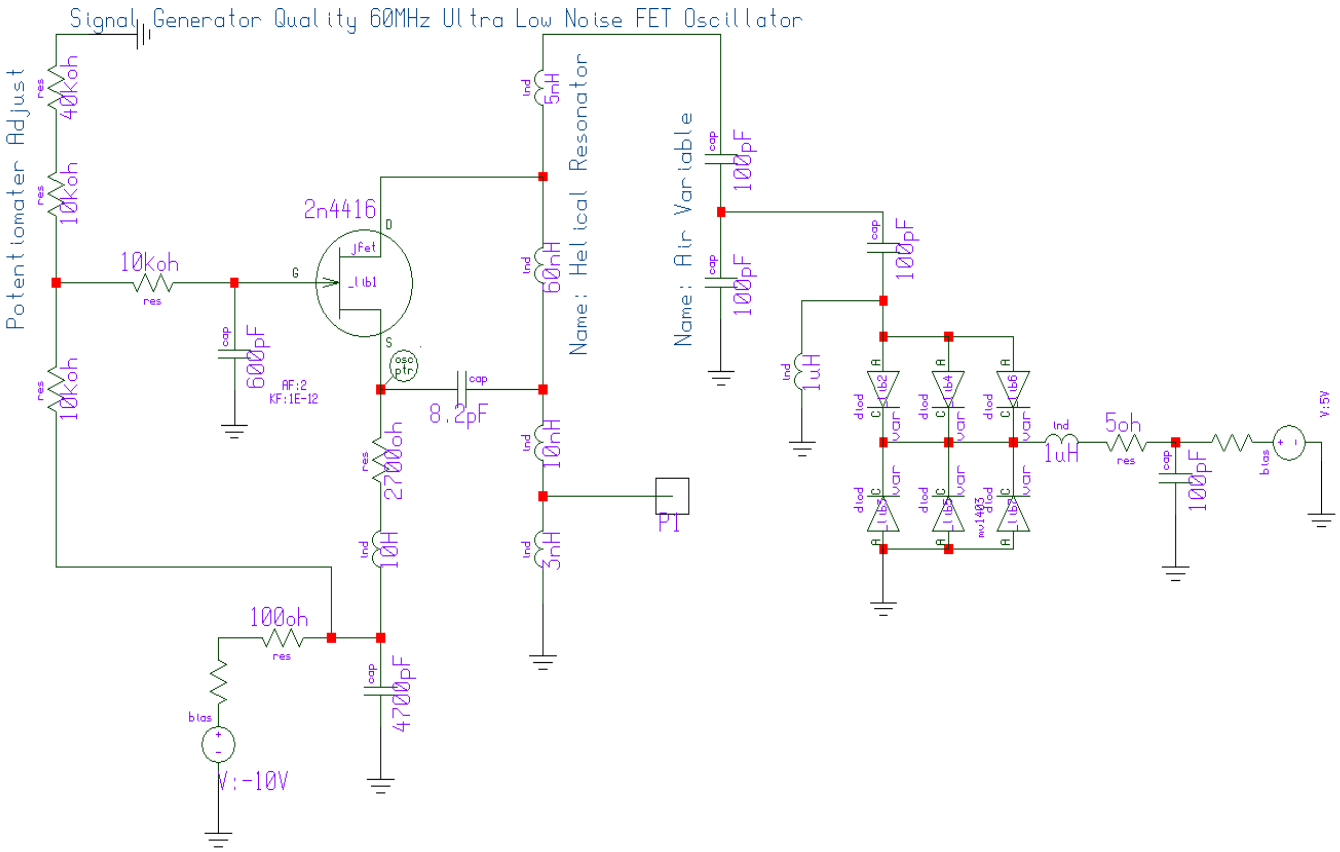


Figure 40: Circuit diagram of the low noise VCO using a 2N4416 FET

It uses a helical resonator, as shown in figure 41. The original cicuit was modified and is using 6 aditional diodes for a wider tuning range , and the parallel combination of the diodes because of no noise cotrrelation result overall in a lower noise contribution

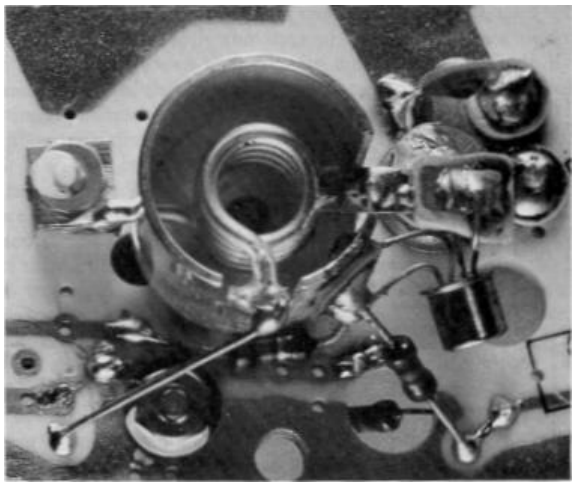


Figure 41: Shows the mechanical implementation of the oscilltor of fig. 40 using a helical resonator [7]

Now the phase noise will be interesting. In practice such an oscillator will have a buffer stage and it was explained above, that the buffer stage will make the far off noise worse so the result will be limited to about –165 dBc/Hz. This oscillator has an output level of 10 dBm (10mW). The theorethical noise limit is 177dB + 10 dB => 187 dBc/Hz. The differenc is due to the large signal noise figure the transistor has.

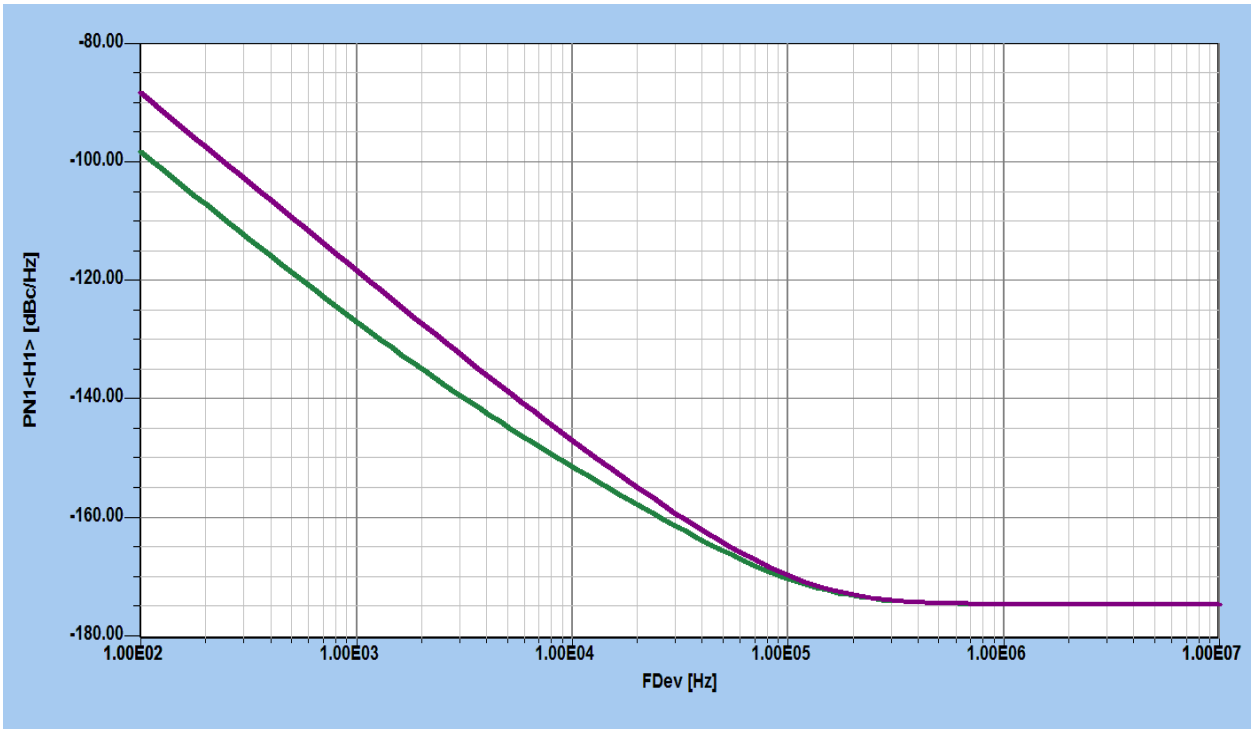


Figure 42: Shows the phase noise simulation of the 60 MHz oscillator using the helical resonator (green trace) and tuning diodes (purple trace).

The diodes makes the VCO noisier below 100KHz, but as the loop bandwidth typically (hopefully) is wider, this compensates the noise . If we look at eqn.8, we will find that the major noise contribution is the loaded Q of the resonator.

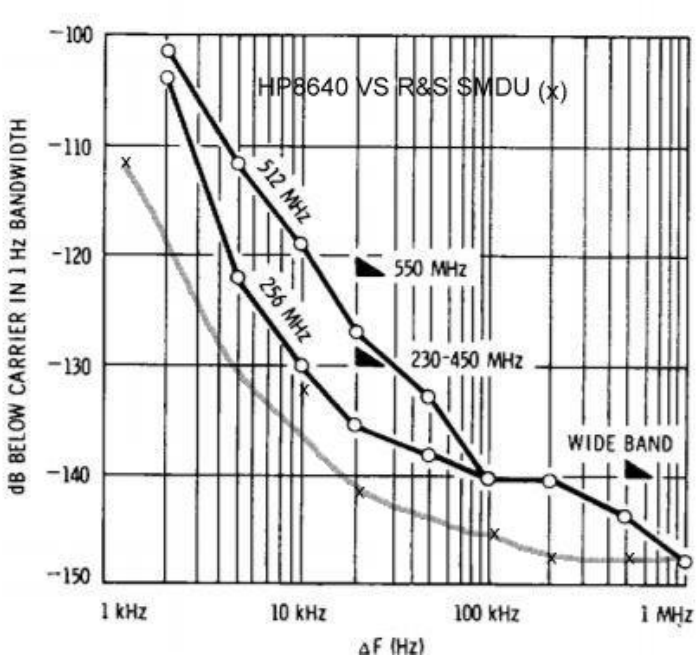


Figure 43: Comparing the phase noise of the HP8640 generator (using a mechanically tuned quarter wave resonator) and the R&S SMDU (helical resonator) tuned with an air variable capacitor

Plot shows superior performance due to the helical resonator in comparison to the mechanically tuned quarter wave resonator, as it can be tapped to achieve better impedance matching.

Principle of a PLL frequency synthesizers [1]

A PLL based frequency synthesizer, see below, is a control system that stabilizes a VCO against a frequency refernce, in this case a crystal oscillator. For a good understanding here is an example. The 2 m radio aamateur frequencies are 144MHz to 148MHz (USA). Let us assume a chanell spacing of 12.5 kHz. In this case the input fom a 10 MHz frequency standard will be divided to 12.5 kHz, this is done by the reference divider R, R=800.

For a center frequency of 146MHz the N divider is set to 1168. The phase frequency detector compares the inupt from the reference divider with the main divider and changes the DC VCO frequency control volatige for the system to be in lock . The loop filter supresses the 12.5 kHz ref. frequency (to a high degree)

This is also the muliplier by which the phase/frequecy detector noise and the refence noise gets multiplied up. Let us assume for a moment that the R divider is the main noise contributor with a noise floor of -150 dBc/Hz . PN=20xlog(N), N=1168. Therefore the noisefloor insider the 146 MHz loop will be 150-81=69 , reduced - 69dB/Hz.

Now to improve this we multiply the ref 10 MHz times 10 to 100Mhz,and in a mixer converter the VCO frequency to 46 Mhz and get much less division, namely N=368. In dB this is 71 dB. The in band phase noise now is 10-71 or 79dB/Hz, a 10dB improvent. This is a very simple example in preparation to explain the fractional syntesizer next. As seen from the block diagram each stage adds noise to the system.

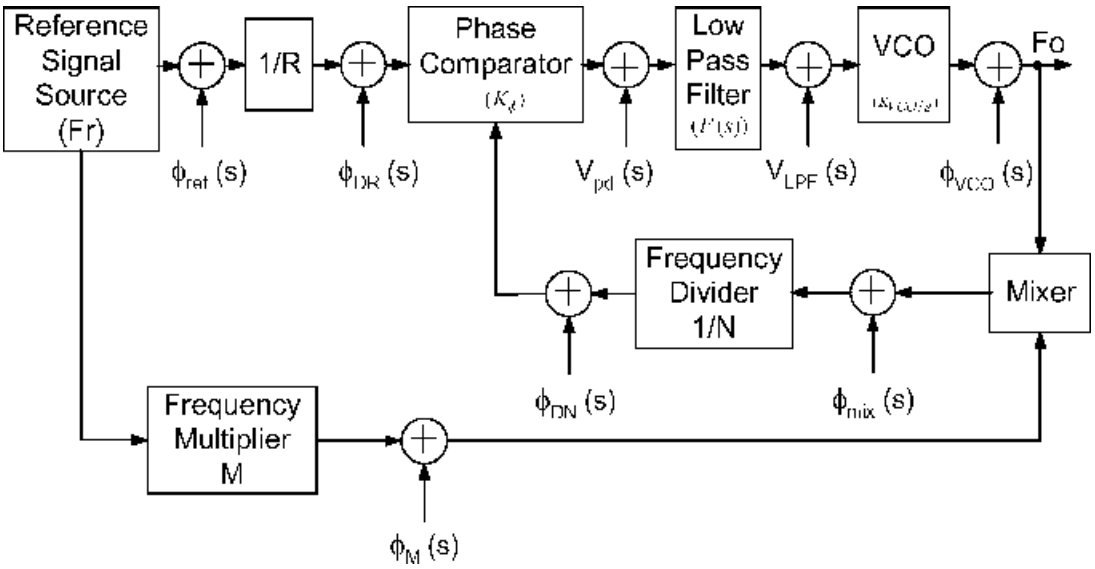


Figure 44: PLL Based Frequency Synthesizer [1]

PLL frequency synthesizers are particularly flexible to use and to be controlled by digital commands. In addition to this they offer many distinct advantages over other forms of local oscillator for many applications both in radio communications equipment as well as test equipment, etc. As a result PLL frequency synthesizers are widely used for many RF applications. Even though other forms of generator including Direct Digital Synthesizers are available, the PLL based synthesizer has many advantages, and can often be used in conjunction with other generators including DDS circuits. The DDS circuits will be described soon. The fractional N synthesizer principle is next.

The Fractional-*N* Principle [1]

The principle of the fractional-*N* PLL synthesizer has been around for a while. In the past, implementation of this has been done in an analog system. It would be ideal to be able to build a single-loop synthesizer with a 1.25-MHz or 50-MHz reference and yet obtain the desired step size resolution, such as 25 kHz. This would lead to the much smaller division ratio and much better phase noise performance.

An alternative would be for *N* to take on fractional values. The output frequency could then be changed in fractional increments of the reference frequency. Although a digital divider cannot provide a fractional division ratio, ways can be found to accomplish the same task effectively.

The most frequently used method is to divide the output frequency by (*N* + 1) every *M* cycles and to divide by *N* the rest of the time. The effective division ratio is then *N* + 1/*M*, and the average output frequency is given by

$$f_o = \left(N + \frac{1}{M} \right) f_r \qquad (25)$$

This expression shows that f_o can be varied in fractional increments of the reference frequency by varying *M*. The technique is equivalent to constructing a fractional divider, but the fractional part of the division is actually implemented using a phase accumulator. The phase accumulator approach is

illustrated by the following example. This method can be expanded to frequencies much higher than 6 GHz using the appropriate synchronous dividers.

Example: Considering the problem of generating 899.8 MHz using a fractional-*N* loop with a 50-MHz reference frequency,

899.8 MHz = 50 MHz $\left(N + \frac{K}{F} \right)$

The integral part of the division *N* has to be set to 17 and the fractional part $\frac{K}{F}$ needs to be $\frac{996}{1000}$; (the fractional part $\frac{K}{F}$ is not an integer) and the VCO output has to be divided by 996 $\times$ every 1000 cycles. This can easily be implemented by adding the number 0.996 to the contents of an accumulator every cycle. Every time the accumulator overflows, the divider divides by 18 rather than by 17. Only the fractional value of the addition is retained in the phase accumulator. If we move to the lower band or try to generate 850.2 MHz, *N* remains 17 and $\frac{K}{F}$ becomes $\frac{4}{1000}$. This method of using fractional division was first introduced by using analog implementation and noise cancellation, but today it is implemented totally as a digital approach. The necessary resolution is obtained from the dual modulus prescaling, which allows for a well-established method for achieving a high-performance frequency synthesizer operating at UHF and higher frequencies. Dual-modulus prescaling avoids the loss of resolution in a system compared to a simple prescaler; it allows a VCO step equal to the value of the reference frequency to be obtained. This method needs an additional counter and the dual modulus prescaler then divides one or two values depending upon the state of its control. The only drawback of prescalers is the minimum division ratio of the prescaler for approximately N^2. The dual modulus divider is the key to implementing the fractional-*N* synthesizer principle. Although the fractional-*N* technique appears to have a good potential of solving the resolution limitation, it is not free of having its own complications. Typically, an overflow from the phase accumulator, which is the adder with the output feedback to the input after being latched, is used to change the instantaneous division ratio. Each overflow produces a jitter at the output frequency, caused by the fractional division, and is limited to the fractional portion of the desired division ratio.

In our case, we had chosen a step size of 200 kHz, and yet the discrete sidebands vary from 200kHz for $\frac{K}{F} = \frac{4}{1000}$ to 49.8MHz for $\frac{K}{F} = \frac{996}{1000}$. It will become the task of the loop filter to remove those discrete spurious. While in the past the removal of the discrete spurs has been accomplished by using analog techniques, various digital methods are now available. The microprocessor has to solve the following equation:

$$N^* = \left(N + \frac{K}{F} \right) = \left[N(F - K) + (N + 1)K \right] \tag{26}$$

Example – To generate 850.2MHz with a 50MHz reference:

For F_O = 850.2 MHz, we obtain:

$$N^* = \frac{850.2\ \mathrm{MHz}}{50\ \mathrm{MHz}} = 17.004$$

Following the formula above:

$$N^* = \left(N + \frac{K}{F} \right) = \frac{\left[17(1000 - 4) + (17 + 1) \times 4 \right]}{1000}$$

$$= \frac{\left[16932 + 72 \right]}{1000} = 17.004$$

$$F_{out} = 50\ \mathrm{MHz} \times \frac{\left[16932 + 72 \right]}{1000}$$

= 846.6 MHz + 3.6 MHz = 850.2 MHz

By increasing the number of accumulators, frequency resolution much below 1-Hz step size is possible with the same switching speed.

There is an interesting, generic problem associated with *all* fractional-*N* synthesizers. Assume for a moment that we use our 50-MHz reference and generate a 550-MHz output frequency. This means our division factor is 11. Aside from reference-frequency sidebands (± 50 MHz) and harmonics, there will be no unwanted spurious frequencies. Of course, the reference sidebands will be suppressed by the loop filter by more than 90 dB. For reasons of phase noise and switching speed, a loop bandwidth of 100 kHz has been considered. Now, taking advantage of the fractional-*N* principle, say we want to operate at an offset of 30 kHz (550.03 MHz). With this new output frequency, the inherent spurious-signal reduction mechanism in the fractional-*N* chip limits the reduction to about 55 dB. Part of the reason why the spurious-signal suppression is less in this case is that the phase-frequency detector acts as a mixer, collecting both the 50-MHz reference (and its harmonics) and 550.03 MHz. Mixing the 11th reference harmonic (550 MHz) and the output frequency (550.03 MHz) results in output at 30 kHz; since the loop bandwidth is 100 kHz, it adds nothing to the suppression of this signal. To solve this, we could consider narrowing the loop bandwidth to 10% of the offset. A 30-kHz offset would equate to a loop bandwidth of 3 kHz, at which the loop speed might still be acceptable, but for a 1-kHz offset, the necessary loop bandwidth of 100 Hz would make the loop too slow. A better way is to use a different reference frequency--one that would place the resulting spurious product considerably outside the 100-kHz loop-filter window. If, for instance, we used a 49-MHz reference, multiplication by 11 would result in 539 MHz. Mixing this with 550.03 MHz would result in spurious signals at ±11.03 MHz, a frequency so far outside the loop bandwidth that it would essentially disappear. Starting with VHF, low-phase-noise crystal oscillator, such as 130 MHz, one can implement an intelligent reference-frequency selection to avoid these discrete spurious signals. An additional method of reducing the spurious contents is

maintaining a division ratio greater than 12 in all cases. Actual tests have shown that these reference-based spurious frequencies can be repeatable suppressed by 80 to 90 dB.

Spur-Suppression Techniques

While several methods have been proposed in the literature, the method of reducing the noise by using a sigma-delta modulator has shown to be most promising. The concept is to get rid of the low-frequency phase error by rapidly switching the division ratio to eliminate the gradual phase error at the discriminatory input. By changing the division ratio rapidly between different values, the phase errors occur in both polarities, positive as well as negative, and at an accelerated rate that explains the phenomenon of high-frequency noise push-up. This noise, which is converted to a voltage by the phase/frequency discriminator and loop filter, is filtered out by the low-pass filter. The main problem associated with this noise shaping technique is that the noise power rises rapidly with frequency. Figure 45 shows noise contributions with such a sigma-delta modulator in place.

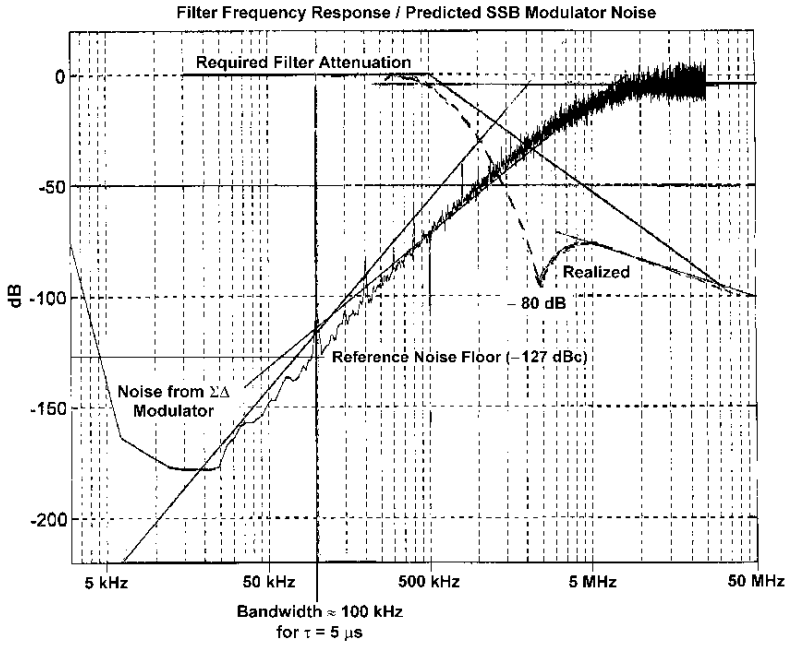


Figure 45: The filter frequency response/phase noise analysis graph shows the required attenuation for the reference frequency of 50 MHz and the noise generated by the sigma-delta converter (three steps) as a function of the offset frequency [1]

It becomes apparent that the sigma-delta converter noise dominates above 80 kHz unless attenuated.

On the other hand, we can now, for the first time, build a single-loop synthesizer with switching times as fast as 6 μs and very little phase-noise deterioration inside the loop bandwidth, as seen in Figure 45. Since this system maintains the good phase noise of the ceramic-resonator-based oscillator, the resulting performance is significantly better than the phase noise expected from high-end signal generators. However, this method does not allow us to increase the loop bandwidth beyond the 100-kHz limit, where the noise contribution of the sigma-delta modulator takes over.

Table 1 shows some of the modern spur-suppression methods. These three-stage sigma-delta methods with larger accumulators have the most potential.

Table 1

Technique	*Feature*	*Problem*
DAC Phase Estimation	Cancel Spur by DAC	Analog Mismatch
Pulse Generation	Insert Pulses	Interpolation Jitter
Phase Interpolation	Inherent Fractional Divider	Interpolation Jitter
Random Jittering	Randomize Divider	Frequency Jitter
Sigma-Delta Modulation	Modulate Division Ratio	Quantization Noise

The power spectral response of the phase noise for the three-stage sigma-delta modulator is calculated from:

$$L(f) = \frac{(2\pi)^2}{12 \cdot f_{ref}} \cdot \left[2\sin\left(\frac{\pi \quad f}{f_{ref}} \right) \right]^{2(n-1)} \quad rad^2 / Hz \qquad (27)$$

where *n* is the number of the stage of the cascaded sigma-delta modulator. Eq. (6-65) shows that the phase noise resulting from the fractional controller is attenuated to negligible levels close to the center frequency, and further from the center frequency, the phase noise is increased rapidly and must be filtered out prior to the tuning input of the VCO to prevent unacceptable degradation of spectral purity. A loop filter must be used to filter the noise in the PLL loop. Figure 45 showed the plot of the phase noise versus the offset frequency from the center frequency. A fractional-*N* synthesizer with a three-stage sigma-delta modulator as shown in Figure 46 has been built. The synthesizer consists of a phase/frequency detector, an active low-pass filter (LPF), a voltage-controlled oscillator (VCO), a dual-modulus prescaler, a three-stage sigma-delta modulator, and a buffer. Figure 47 shows the inner workings of the chip in greater detail.

After designing, building, and predicting the phase noise performance of this synthesizer, it becomes clear that the measuring of the phase noise of such a system becomes tricky. Standard measurement techniques that use a reference synthesizer would not provide enough resolution because there are no synthesized signal generators on the market sufficiently good enough to measure such low values of phase noise. Therefore, we had to build a comb generator that would take the output of the oscillator and multiply this up 10 to 20 times.

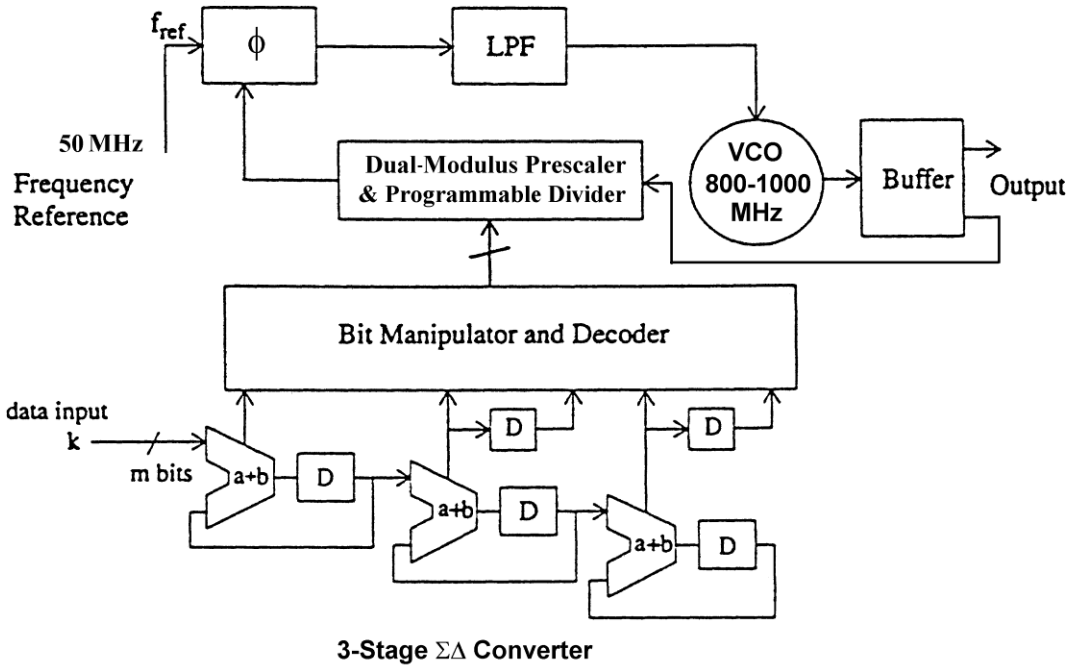


Figure 46: Fractional-N Division Synthesizer [1]

The Frac-N is found mostly in very low power applications like portable two way radios but circuits with DDS designs are taken over for high performance applications.

The next diagram shows the block diagram of a typical commercially available Frac-N IC from Analog Devices.

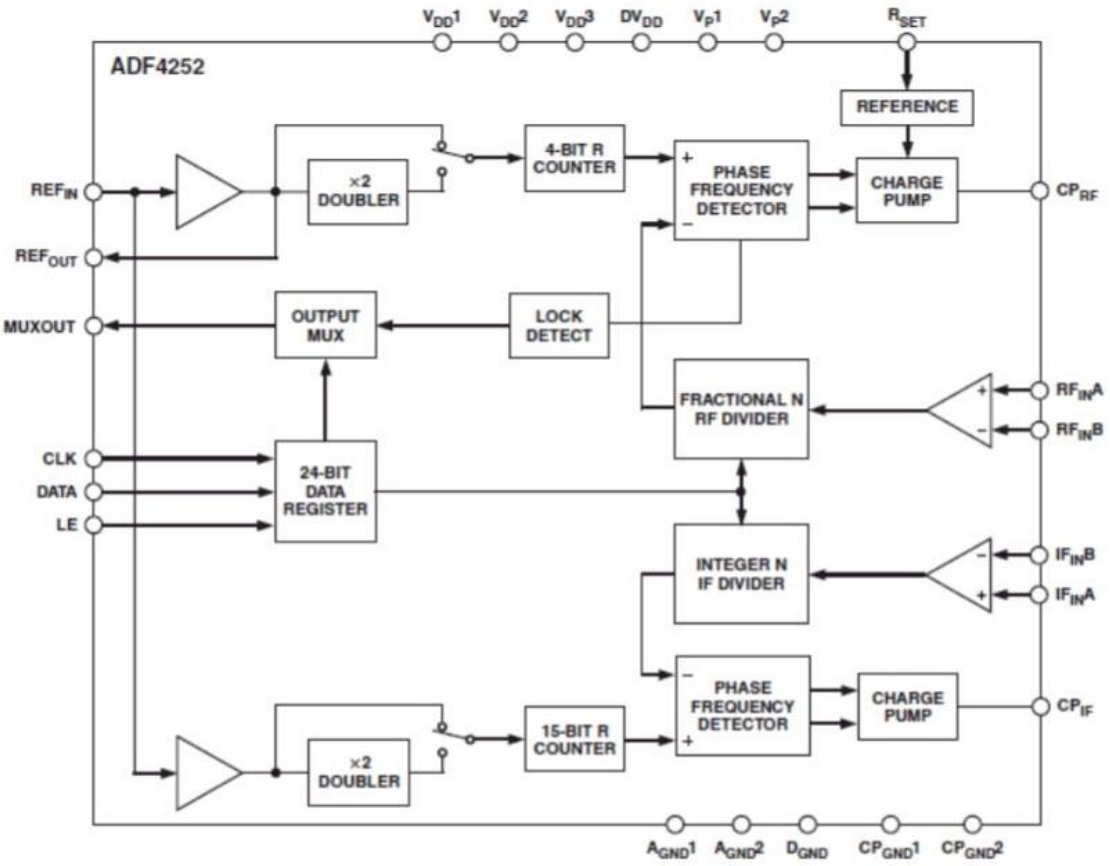


Figure 47: Typical Commercially available Frac-N IC ADF4252

Now, some examples for single or dual loop PLL stages for best phase noise:

The following are examples of high Q resonators locked against a simple PLL. The configuration of each case is explained. They are oscillators as used as auxiliary frequency sources in generators.

First Loop: Internal 800 MHz SAW Oscillator locked to 10 MHz, PLL IC is HMC698 Integer N

Second Loop: 13.5 GHz DRO locked to 800 MHz SAW, PLL IC is RFDIV3 IC

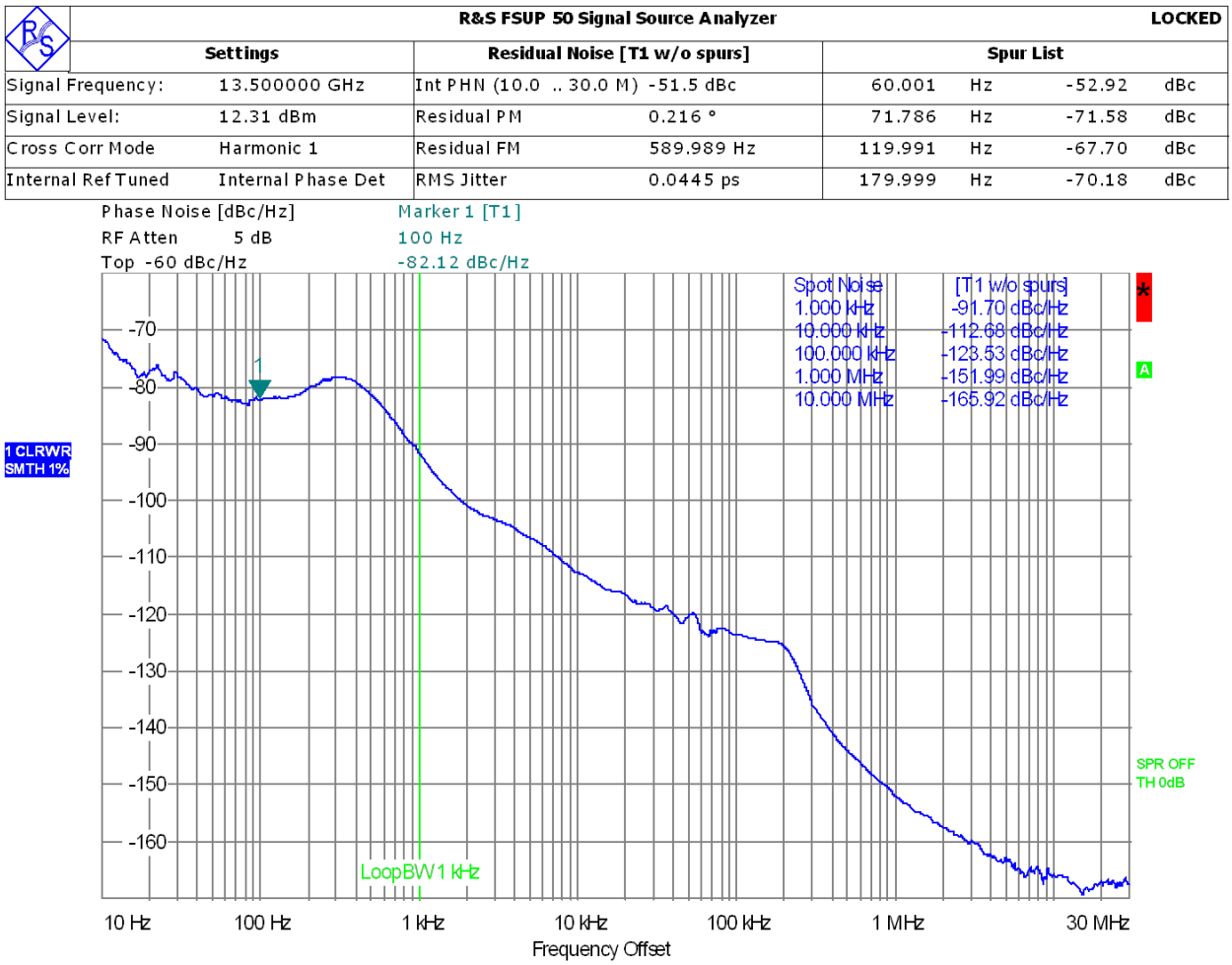


Figure 48: 13.5 GHz Dual Loop Synthesizer

Single Loop phase locked DRO, 1280 MHz reference

12.8 GHz DRO locked to 1280 MHz, PLL IC is RFDIV3

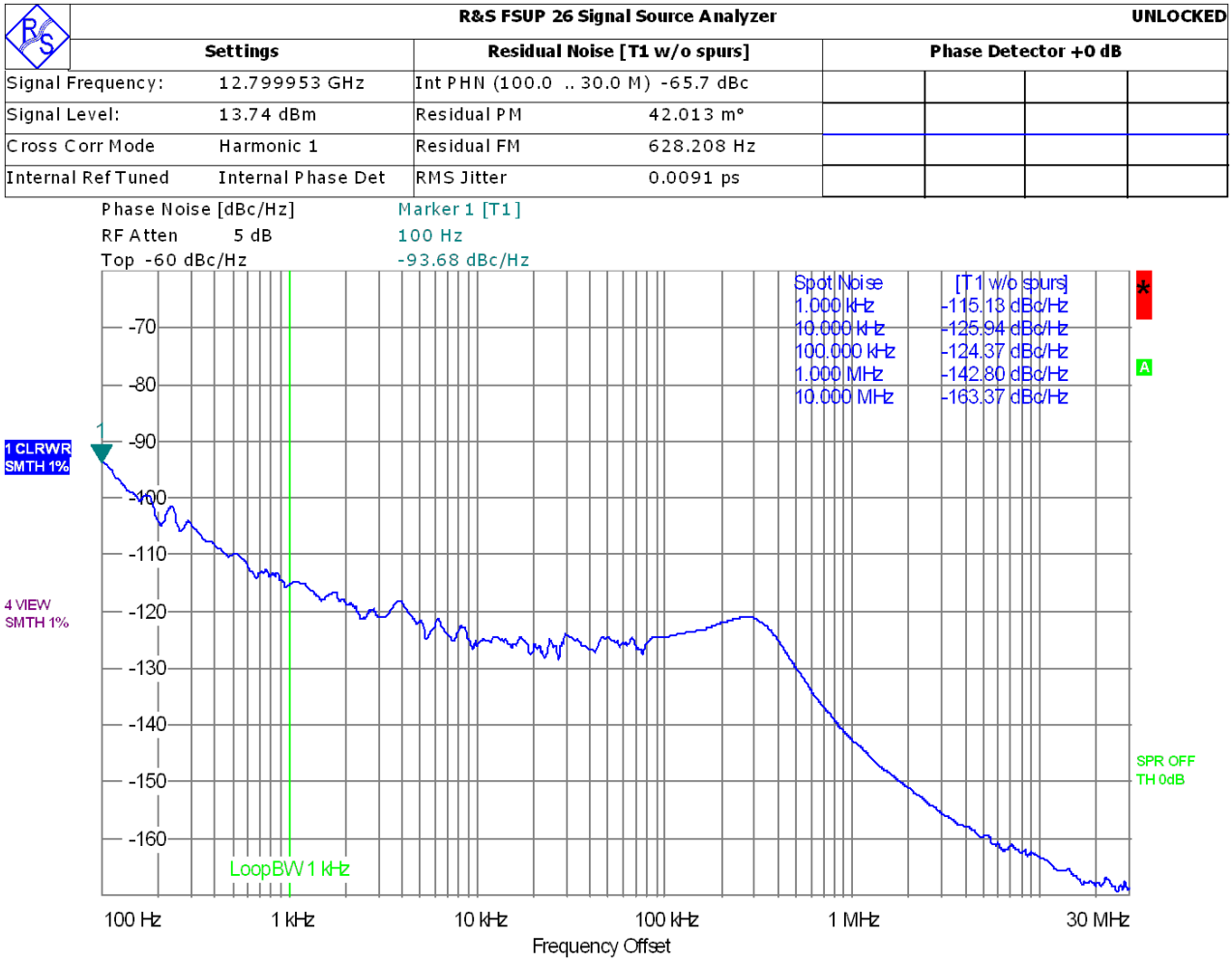


Figure 49: Single Loop phase locked DRO, 1280 MHz reference

FSFLO13G00-100-1

Single Loop phase locked VCO, 100 MHz reference

100 MHz multiplied by 8, 13 GHz is locked to 800 MHz. PLL IC is RFDIV3

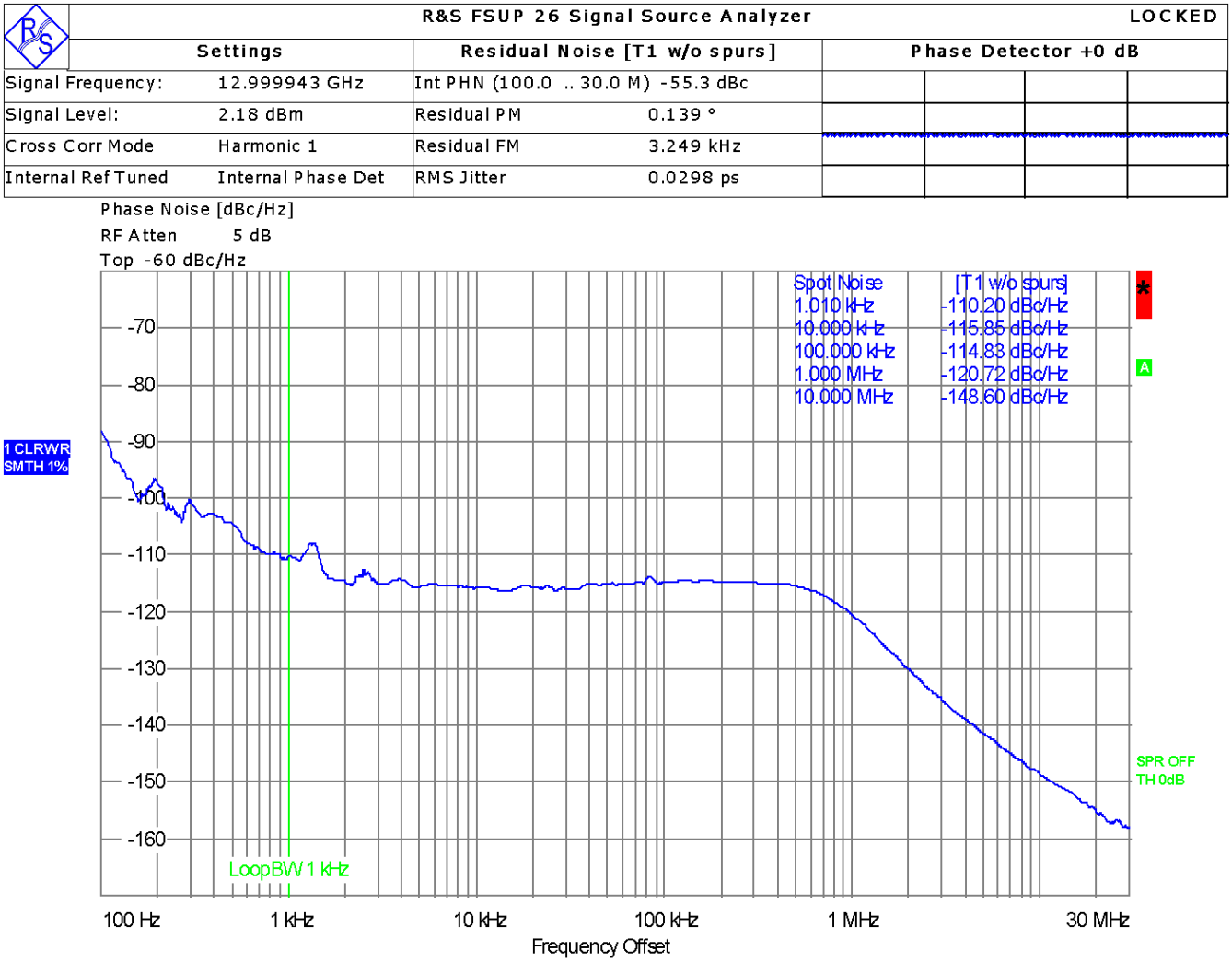


Figure 50: Single Loop Frac-N phase locked 13GHz VCO with 100 MHz reference

KSFLO27R1-12-100

Single Loop phase locked VCO, 100 MHz reference

Comparison frequency is 100MHz, PLL IC is HMC703 Fractional N synthesizer. VCO output at 13.55 GHz, followed by a doubler.

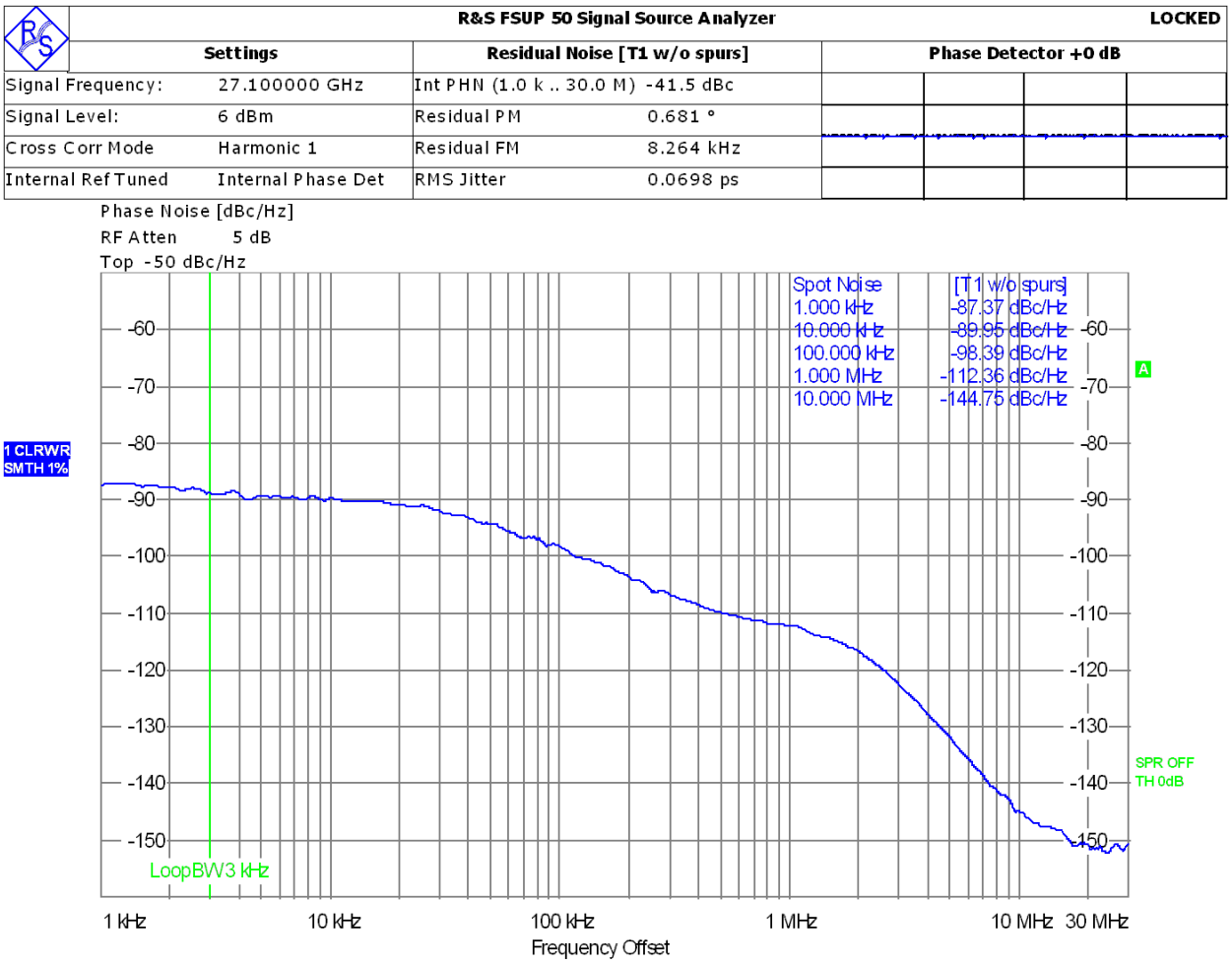


Figure 51: Single Loop Frac-N phase locked VCO with 100 MHz reference

Phase locked SAW oscillator at 1 GHz.

The trick used in here is that both a mixer and a PLL IC are used to control the SAW oscillator. The PLL IC (ADF4106) is used to provide frequency lock, and the mixer is used to clean up the phase noise.

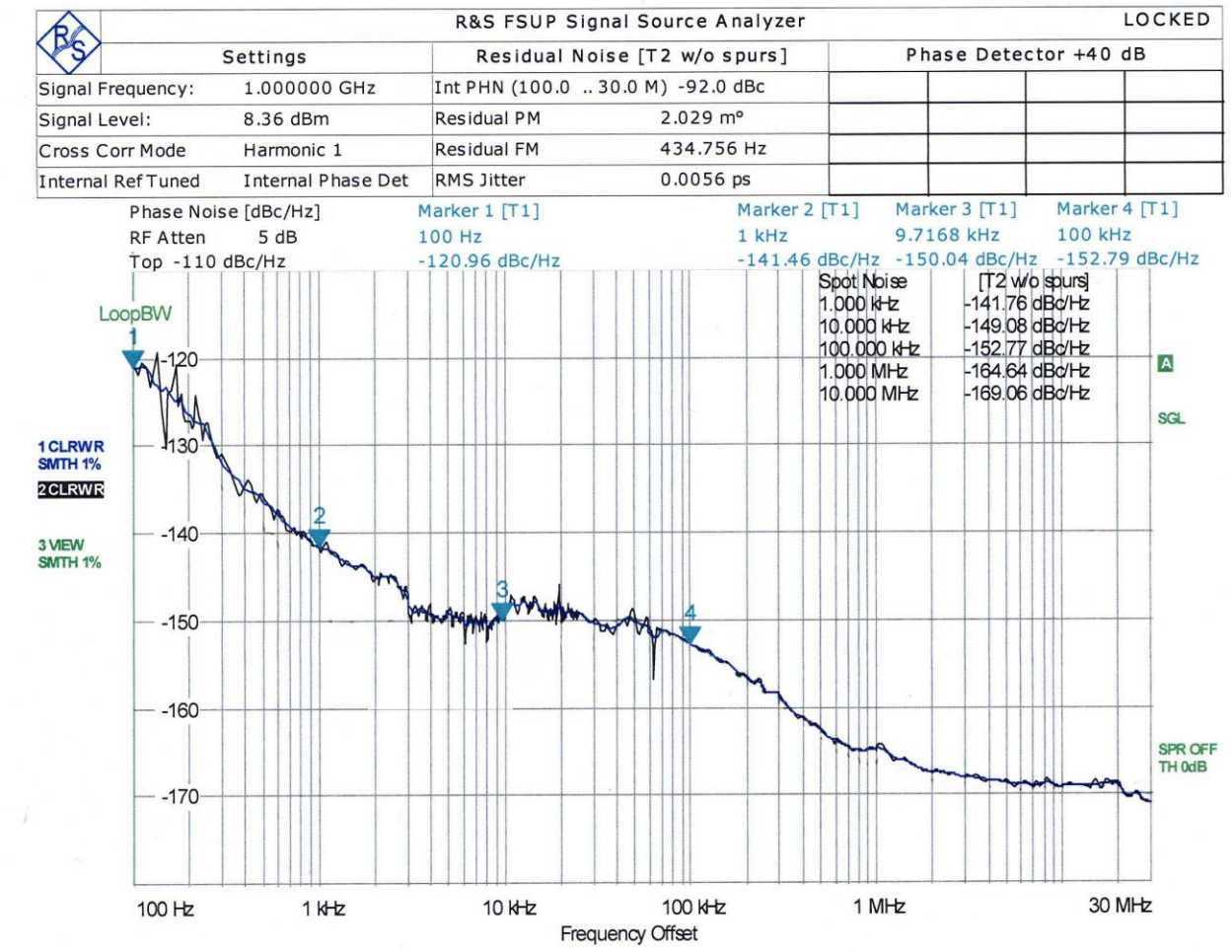


Figure 52: Phase locked SAW oscillator at 1 GHz

We have now looked at the oscillators (VCO'S) used in signal generators and at some fixed frequency oscillators. The YIG design on purpose was not yet included. To make a signal generator from an oscillator, a set of output stages are missing, including the programmable attenuator, the FM modulation capability and the AM modulation capability, placed somewhat towards the output. The FM modulations as mentioned, both analog modulation must have very low distortion.

The following block diagrams are part of one of the last analog signal generators, we were now looking at the transition from the conventional designs to the more advanced circuits with DDS and wide band modulation capabilities.

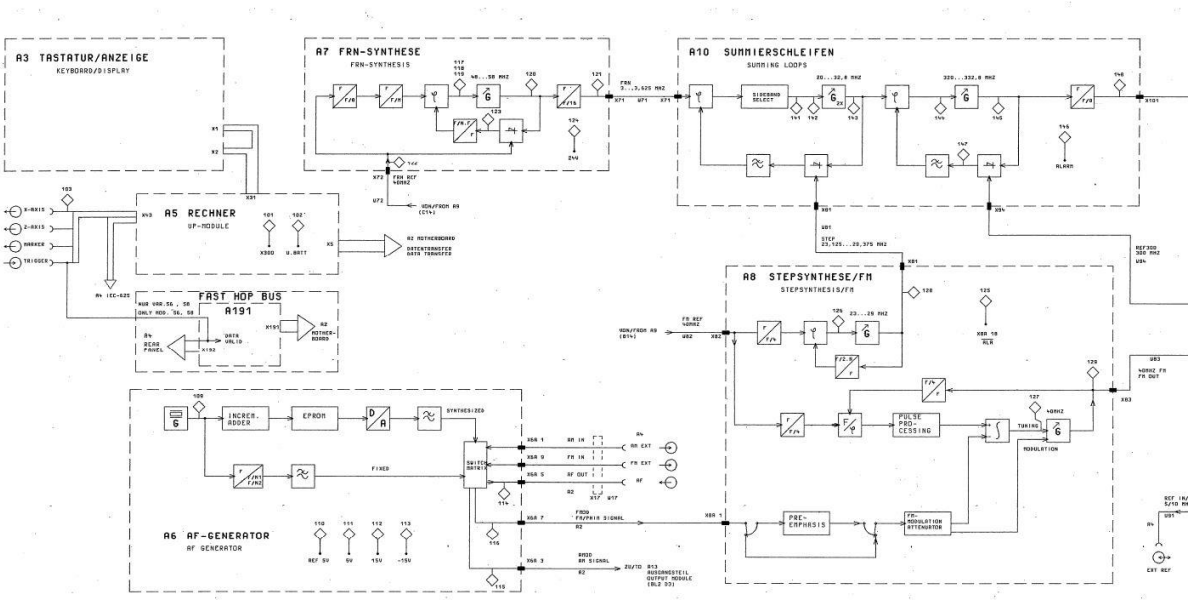


Figure 53: The main systhesizer part of a "traditional" signal generator

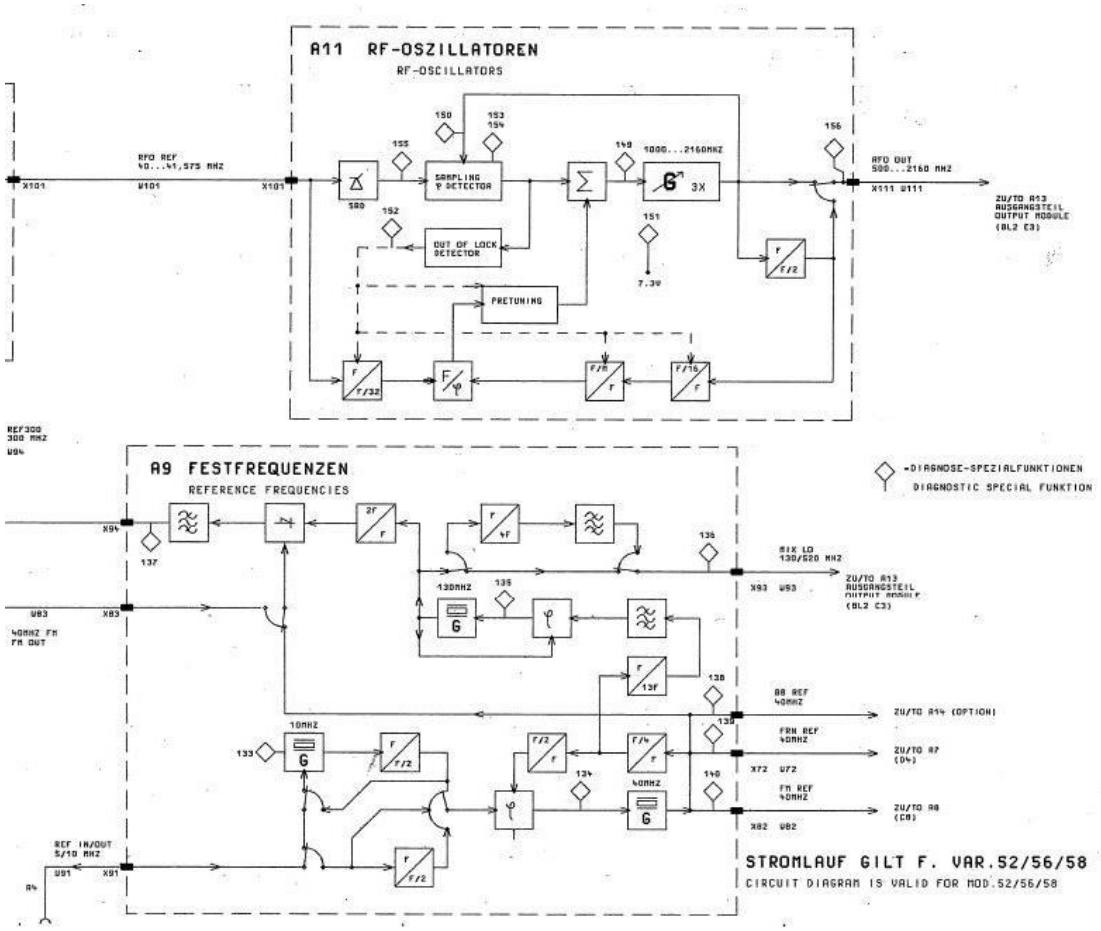


Figure 54: Generation of reference frequency stages (variable and fixed)

Already these “analog” signal generators used a sophisticted method for I&Q modulation, shown below (See Minimum Shift Keying option).

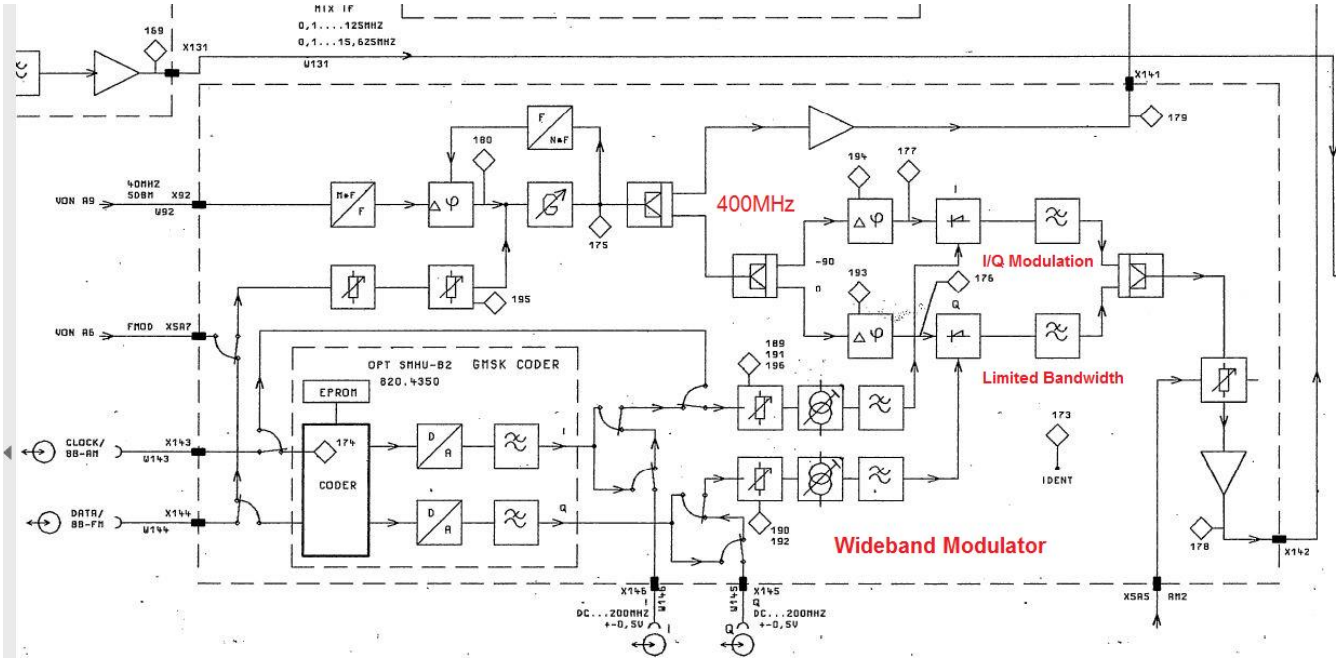


Figure 55: WideBand Modulators

Generating Auxiliary Frequencies with Low Phase Noise

In a conventional signal generator, a variable frequency reference is supplied to a phase-locked oscillator, which is then excited into oscillation at an adjustable frequency. A high-frequency generator may also be built around a switchable phase-locked loop. The output signal of the oscillator is supplied optionally to a frequency splitter or a series circuit of several mixers. The output of the frequency splitter is used to adjust the oscillator to a coarse frequency. In order to implement a fine adjustment, the system then switches to the output of the series-connected mixers. Unfortunately, in a signal generator of this design, it is difficult to achieve low phase noise. [5]

A high frequency signal generator that achieves very good secondary-line spacing with low phase noise is described in [5]. It comprises two oscillators locked by means of phase-locked loops (PLL). The first PLL generates a high-quality reference frequency, which can be tuned in small, discrete steps over approximately 10% of the operating frequency. With this restricted frequency range, a high performance voltage-controlled oscillator (VCO) can be constructed. With the use of a frequency splitter outside the PLL, the phase noise of an original fixed-frequency reference signal is largely preserved. The comparison frequency is advantageously around >10 MHz, so that rapid frequency changes are possible. Passive doubling stages with subsequent filtering are used in order to realize extremely low-noise operation. As a result of the filters between the doubling stages, undesirable harmonics are suppressed.

To allow the mixing-down of the VCO to the output frequency with different harmonics of the reference frequency, bridgeable mixers connected in a cascade are used. The output of the oscillators can be mixed down with the different reference signals dependent upon the position of the bridging switch. This frequency range can be further increased by using the mirror signal of the first mixer. The resulting

intermediate frequency is synchronized with a digital phase detector to a fraction of the reference frequency.

Using the reference signal as an input signal for the splitter means that the cross-products do not occur in the mixers. The mixing products are advantageously disposed on a matrix that corresponds to the last intermediate frequency divided by the resolution of the splitter. Through an appropriate choice of the splitting factors, these mixing products can be selected in such a manner that they are suppressed by the loop filter and accordingly no secondary lines occur in the synthesizer.

To allow a very rapid frequency change, the oscillator is pre-tuned based upon an individually measured characteristic of the oscillator.

Detailed Description

An example implementation of the low phase noise high frequency signal generator is shown in Figure 56(a). The system comprises a reference-frequency generator (Figure 56a) and a high-frequency generator (Figure 56b). The reference generator produces a variable reference frequency and supplies it to the high-frequency generator. The high-frequency generator PLL produces a high-frequency signal from the variable reference input. The PLL comprises at least one first mixer, a second mixer, and several switches. The first mixer, the second mixer, and the switches are connected in series. The mixers are connected into the PLL individually in a selective manner by the switches, as shown. Accordingly, an adjustable output frequency is achieved with very low phase noise. The phase noise can be further reduced by lowpass filters after each mixer.

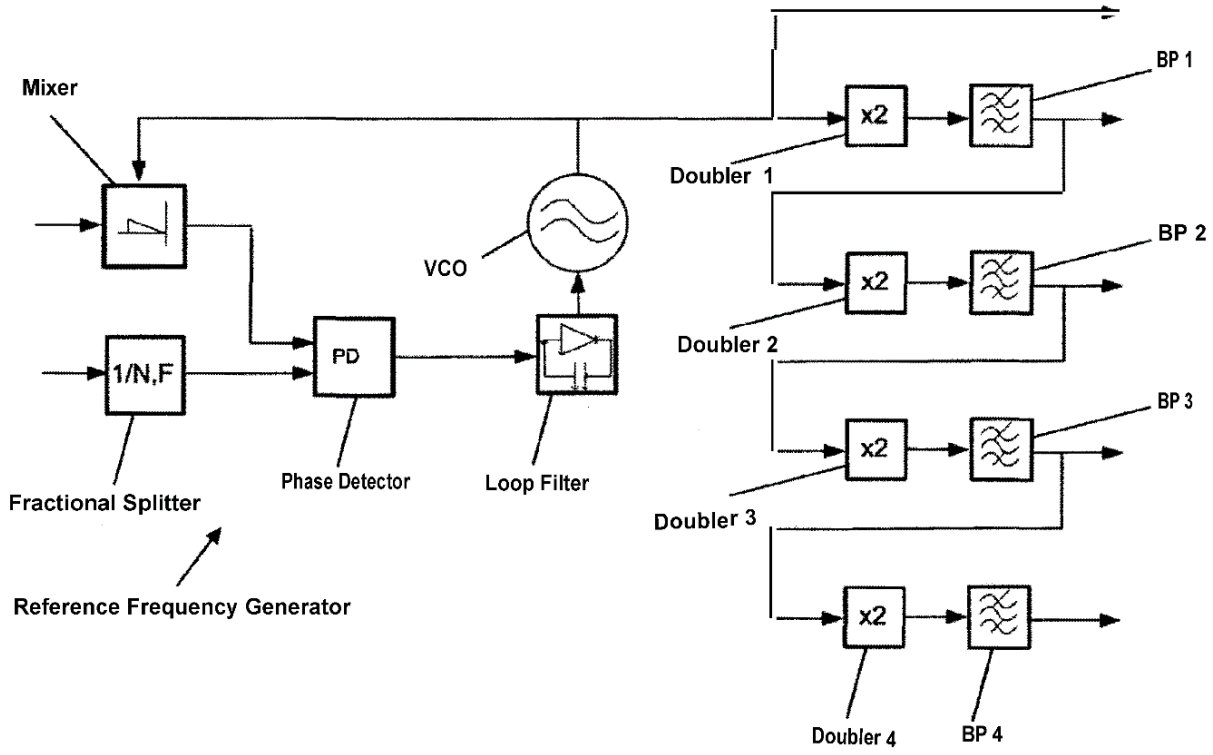
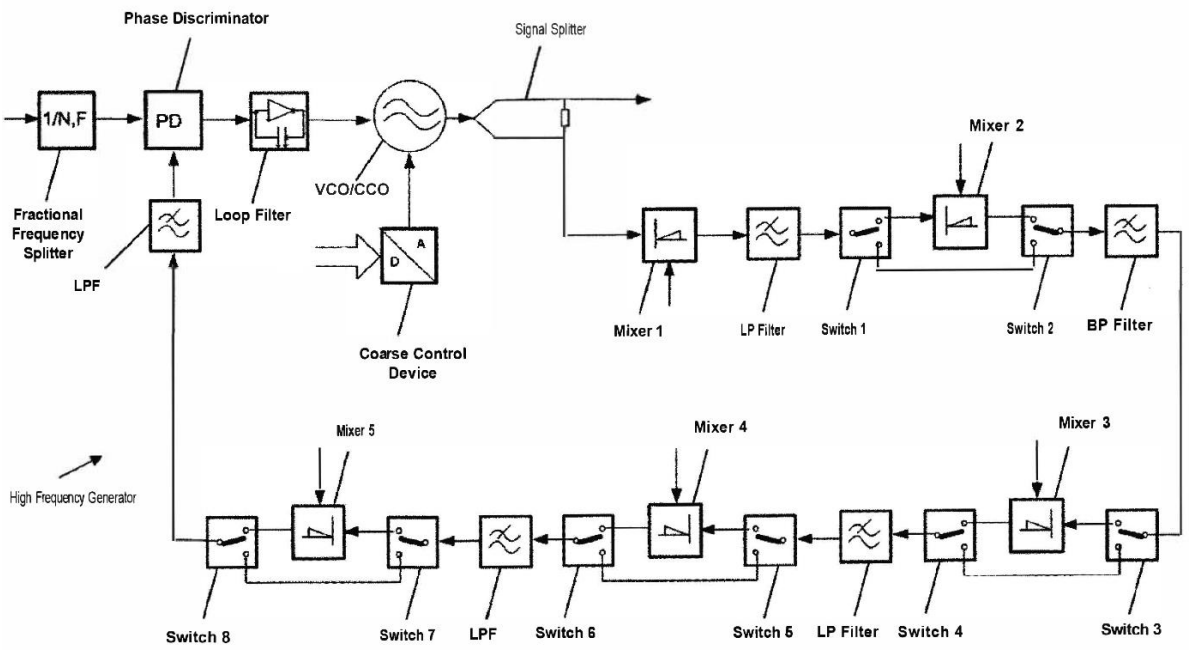


Figure 56(a): Block Diagram of a Reference Frequency Generator [5]



(*b*)

Figure 56(b): Simplified block diagram of the low phase noise high frequency signal generator. (After Alexander Roth, R&S) [5]

As shown in Figure 56a, the reference generator contains a fractional frequency splitter, phase detector, loop filter, VCO, and mixer. A stable frequency reference signal of, for example, 640 MHz, is supplied to the fractional frequency splitter, which generates a signal with a frequency divided by N_{Fref} and supplies it to the phase detector. The phase detector compares this signal with a signal generated by the mixer and outputs a corresponding signal to the loop filter, which transmits it to the VCO. This generates an output signal of, for example, 650 MHz–700 MHz, and supplies it again to the mixer, where it is mixed with a stable-frequency reference signal.

In the case of a reference signal of, for example, 640 MHz, an output signal of the mixer of 10 MHz–60 MHz is obtained. The frequency of the output signal of the VCO is accordingly adjusted by setting the splitting factor N_{Fref} of the fractional splitter.

The reference-frequency generator further comprises four frequency doublers, each of which doubles the frequency of the input signal. A bandpass filter, which in each case allows only the doubled frequency to pass and filters out other components of the signals, is connected downstream of each frequency doubler. Accordingly, a reference frequency signal of 650 MHz–700 MHz in the example is present at the output of the voltage-controlled oscillator. It follows that:

- A doubled reference frequency of 1.3–1.4 GHz is present at the output of bandpass filter 1.
- A quadrupled reference frequency of 2.6–2.8 GHz is present at the output of bandpass filter 2.
- An 8-fold reference frequency of 5.2–5.6 GHz is present at the output of bandpass filter 3.
- A 16-fold reference frequency of 10.4–11.2 GHz is present at the output of bandpass filter 4.

The doubled reference frequency of 1.3–1.4 GHz is supplied to a fractional frequency splitter (Figure 56b) that divides the signal by a factor of N_{Fmain}. By multiplying the frequency of the reference signal in small steps with subsequent filtering, it is possible to achieve very low phase noise of the reference.

The output signal of the fractional frequency splitter is supplied to a phase discriminator, which compares it with the signal of the PLL and routes a corresponding output to a loop filter, and then passes it to a voltage-controlled or current-controlled oscillator (CCO), preferably an yttrium-iron-garnet (YIG) oscillator. The signal at the loop filter is used for fine adjustment of the frequency of the controlled oscillator.

A signal is supplied from a coarse-control device to the controlled oscillator for coarse adjustment of the output frequency. The output signal of the VCO is supplied to the PLL via a signal splitter. The VCO output initially passes through Mixer 1, where it is mixed with the 16-fold reference frequency. The output of the mixer is applied to a lowpass filter, which allows only the lower mixing product to pass. This signal is applied to Switch 1, which optionally applies it to Mixer 2 or bridges the mixer. If the signal is applied to Mixer 2, it is combined with the 8-fold reference frequency of 5.2–5.6 GHz in the example. Switch 2, together with Switch 1, implements the switching or the bridging function.

The resulting signal is applied to a bandpass filter, which allows only the lower product of the mixer to pass. If Mixer 2 has been bridged, the low-pass filter plays no role. The output is next applied to the combination of Switch 3 and Switch 4, which either apply the signal to Mixer 3 or bridge it. If the signal is applied to Mixer 3, it is combined with the 4-fold reference frequency of 2.6–2.8 GHz in the example. The output signal is again applied to a lowpass filter, which once again allows only the lower mixing product to pass. Here also, the filter plays no role if Mixer 3 has been bridged.

Switches 5 and 6, Mixer 4 and a lowpass filter form another corresponding functional unit. Mixer 4 combines the input signal with the doubled reference frequency of 1.3–1.4 GHz in the example.

Switches 7 and 8, Mixer 5 and a lowpass filter form yet another corresponding functional unit. Mixer 5 combines the input signal with an unchanged reference frequency of 650–700 MHz in the example. The signal resulting after the lowpass filter is applied to the phase discriminator.

The signals with which the mixers combine the signal of the phase-locked loop are taken from the reference frequency generator (Figure 56a). Mixer 1 can also be advantageously provided with switches, in which case the mixer can also be bridged. As an alternative, a larger or smaller number of mixers can be used in the PLL system. The higher the tuning range of the oscillator, the more mixers are used. [5]

Determination of Splitting Factors

The splitting factors N_{Fref} and N_{Fmain} of the fractional splitters are adjusted in order to achieve the desired output frequency of the oscillator. An output frequency of, for example, 10000 MHz to 18000 MHz is taken as a starting point. Initially, the parameter *V* is calculated, which corresponds to the multiple of the reference frequency f_{ref} with which the mixing-down is to be implemented. The minimal adjustable reference frequency of 650 MHz in the example and an intermediate frequency of, for example, 55 MHz (which is favorable for the main loop), are used as a basis.

$$V = \mathrm{INT}\left(\left(f_{osz} + 55\,\mathrm{MHz}\right) / 650\,\mathrm{MHz}\right) \tag{28}$$

Next, the reference frequency f_{ref} is calculated. For this purpose, the previously determined *V* is used. Because *V* is rounded down to whole numbers, a reference frequency somewhat higher than 650 MHz is obtained.

$$f_{ref} = \left(f_{osz} + 55\,\mathrm{MHz} \right) / V \qquad (29)$$

The value of the splitter of the reference-frequency generator is next calculated. The splitting factor N_{Fref} of the reference-frequency generator is rounded in such a manner that no secondary lines occur within the loop band-width.

$$N_{Fref} = 640\,\mathrm{MHz} / \mathrm{ABS}\left[\left(640 - f_{ref} \right) \right]$$

with rounding to 1/*F* and

F = 8 for *N*<20

F = 4 for 20≤*N*<40

F = 2 for 40≤*N*<80

F = l for 80≤*N*

The rounding to different 1/*F* values prevents the modulation from falling below 8 MHz by a decimal component and accordingly being attenuated by the phase-locked loop.

Next, the intermediate frequency f_{zf} in the PLL of the high frequency generator is calculated. Through the rounding of the splitter in generating the reference frequency f_{ref}, an intermediate frequency f_{zf}, which differs from the set value, is obtained.

$$f_{zf} = V * 640\,\mathrm{MHz} * \left(1 - 1 / N_{Fref} \right) - F_{osz} \qquad (30)$$

This calculated intermediate frequency f_{zf} is now rounded to an adjustable value.

$$N_{Fmain} = 2 * 640\,\mathrm{MHz} * \left(1 - 1 / N_{Fref} \right) / f_{zf} \qquad (31)$$

with rounding of the splitting factor to 1/*F* and

F = 16 for *N*<l0

F = 8 for 10≤*N*<20

F = 4 for 20≤*N*<40

F = 2 for 40≤*N*<80

F = l for 80≤*N*

The rounding to different 1/*F* values prevents the modulation from falling below approximately 8 MHz by the decimal component. The resulting secondary lines are accordingly suppressed by the PLL of the high-frequency generator.

Finally, the actual frequency f_{osz} of the VCO of the high-frequency generator is calculated.

$$f_{osz} = V * 640\,\mathrm{MHz} * \left(1 - 1 / N_{Fref} \right) - \left(2 * 640\,\mathrm{MHz} * \left(1 - 1 / N_{Fref} \right) / N_{Fmain} \right) \qquad (32)$$

The residual error, which arises from rounding the splitting factors N_{Fref}, N_{Fmain}, is smaller than 1 MHz and can be tolerated. With the advantageous use of a direct-digital synthesizer in the PLL of the high-frequency oscillator instead of the fractional splitter, an arbitrary frequency resolution is possible. [5]

Now we move to the important mostly digital frequency generation domain

Part II

Overview: Direct Digital Synthesizers [9-13]

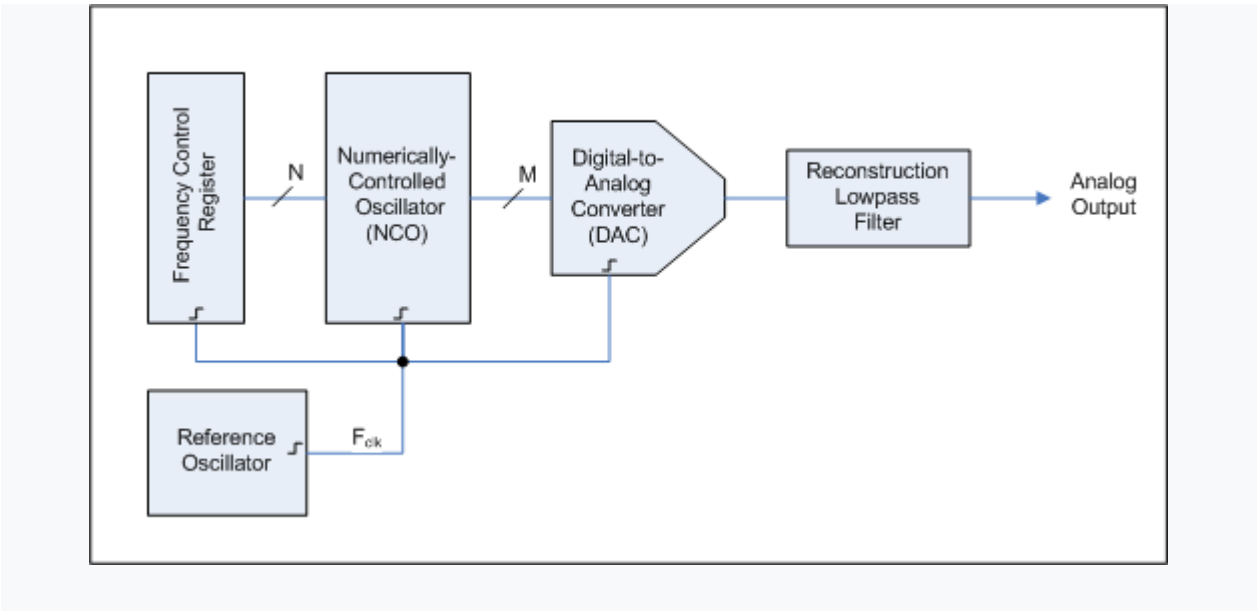


Figure 57: Direct Digital Synthesizer block diagram

A basic Direct Digital Synthesizer consists of a frequency reference (often a crystal or SAW oscillator), a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC) as shown in Figure 57.

The reference oscillator provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the *NCO* which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the *Frequency Control Register*. The sampled, digital waveform is converted to an analog waveform by the *DAC*. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

Performance

A DDS has many advantages over its analog counterpart, the phase-locked loop (PLL), including much better frequency agility, improved phase noise, and precise control of the output phase across frequency switching transitions. Disadvantages include spurs due mainly to truncation effects in the NCO, crossing spurs resulting from high order (>1) Nyquist images, and a higher noise floor at large frequency offsets due mainly to the Digital-to-analog converter.

Because a DDS is a sampled system, in addition to the desired waveform at output frequency F_{out}, Nyquist images are also generated (the primary image is at F_{clk}-F_{out}, where F_{clk} is the reference clock frequency). In order to reject these undesired images, a DDS is generally used in conjunction with an analog reconstruction lowpass filter as shown in Figure 57.

Frequency agility

The output frequency of a DDS is determined by the value stored in the frequency control register (FCR) (see Fig.57), which in turn controls the NCO's phase accumulator step size. Because the NCO operates in the discrete-time domain, it changes frequency instantaneously at the clock edge coincident with a change in the value stored in the FCR. The DDS output frequency settling time is determined mainly by the phase response of the reconstruction filter. An ideal reconstruction filter with a linear phase response (meaning the output is simply a delayed version of the input signal) would allow instantaneous frequency response at its output because a linear system cannot create frequencies that are not present at its input.

Phase noise and jitter

The superior close-in phase noise performance of a DDS stems from the fact that it is a feed-forward system. In a traditional phase locked loop (PLL), the frequency divider in the feedback path acts to multiply the phase noise of the reference oscillator and, within the PLL loop bandwidth, impresses this excess noise onto the VCO output. A DDS on the other hand, reduces the reference clock phase noise by the ratio because its output is derived by fractional division of the clock. Reference clock jitter translates directly to the output, but this jitter is a smaller percentage of the output period (by the ratio above). Since the maximum output frequency is limited to, the output phase noise at close-in offsets is always at least 6dB below the reference clock phase-noise.[6]

At offsets far removed from the carrier, the phase-noise floor of a DDS is determined by the power sum of the DAC quantization noise floor and the reference clock phase noise floor.

Analog Devices MT-085 TUTORIAL:

Fundamentals of the DDS Architecture:

With the widespread use of digital techniques in instrumentation and communications systems, a digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The basic architecture is shown in Figure 58. In this simplified model, a stable clock drives a programmable-read-only-memory (PROM) which stores one or more integral number of cycles of a sinewave (or other arbitrary waveform, for that matter). As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a DAC which in turn generates the analog output signal. The spectral purity of the final analog output signal is determined primarily by the DAC. The phase noise is basically that of the reference clock.

Because a DDS system is a sampled data system, all the issues involved in sampling must be considered: quantization noise, aliasing, filtering, etc. For instance, the higher order harmonics of the DAC output frequencies fold back into the Nyquist bandwidth, making them unfilterable, whereas, the higher order harmonics of the output of PLL-based synthesizers can be filtered. There are other considerations which will be discussed shortly.

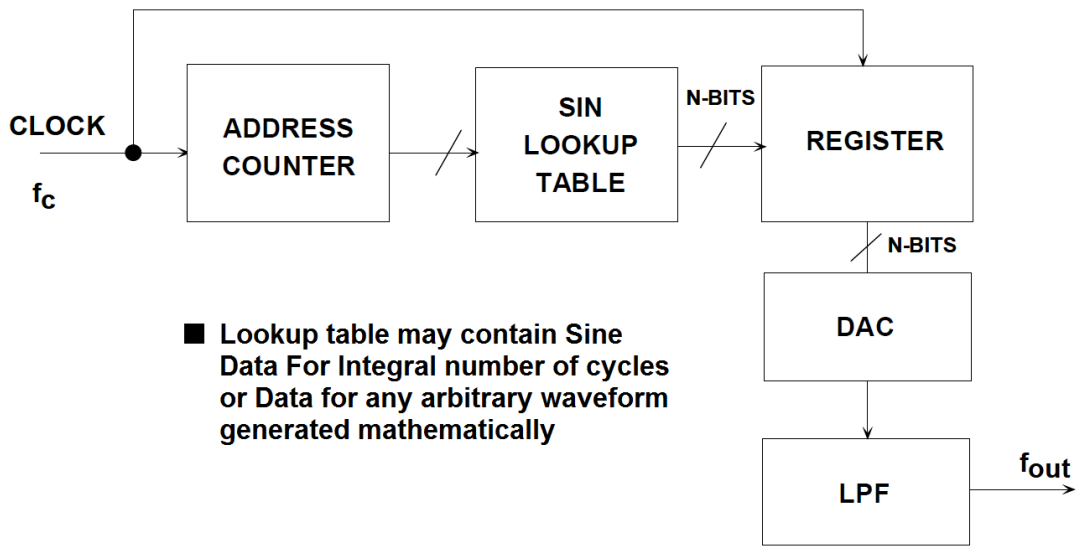


Figure 58: Fundamental Direct Digital Synthesis System [13]

A fundamental problem with this simple DDS system is that the final output frequency can be changed only by changing the reference clock frequency or by reprogramming the PROM, making it rather inflexible. A practical DDS system implements this basic function in a much more flexible and efficient manner using digital hardware called a Numerically Controlled Oscillator (NCO). A block diagram of such a system is shown in Figure 59.

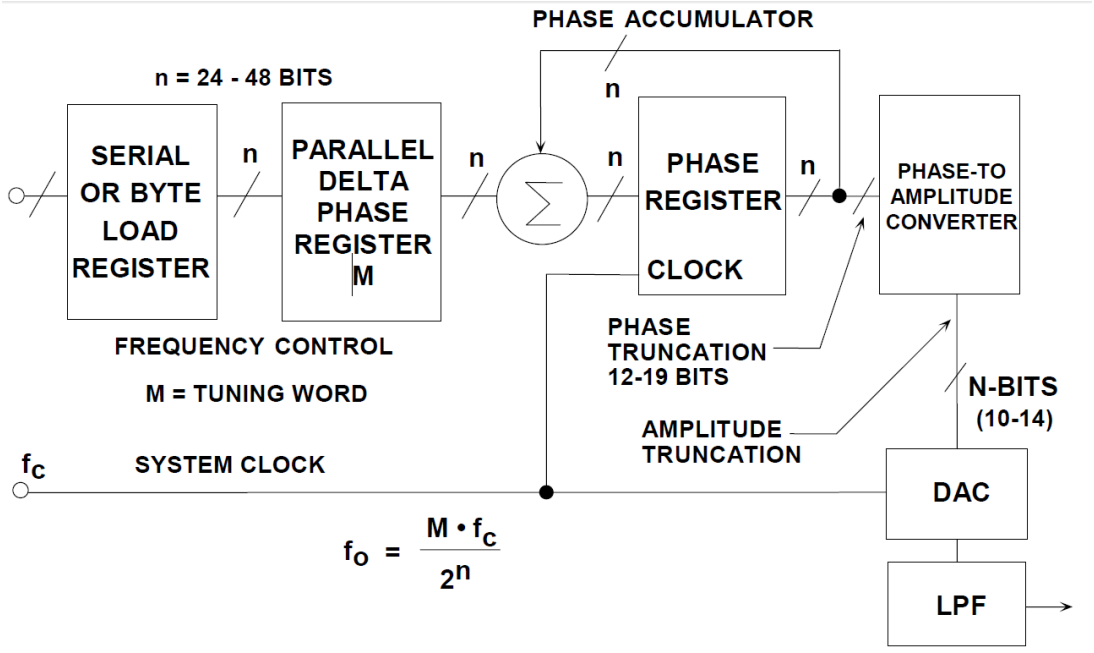
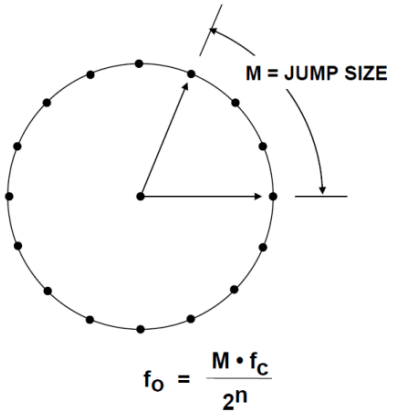


Figure 59: A Flexible DDS System [13]

The heart of the system is the *phase accumulator* whose contents are updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M, stored in the *delta phase register* is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00...01 and that the initial contents of the phase accumulator are 00...00. The phase accumulator is updated by 00...01 on each clock cycle. If the accumulator is 32-bits wide, 232 clock cycles (over 4 billion) are required before the phase accumulator returns to 00...00, and the cycle repeats.

The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sinewave. (Actually, only data for 90° is required because the quadrature data is contained in the two MSBs). The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC. This is shown graphically using the "phase wheel" in Figure 60.

Consider the case for n = 32, and M = 1. The phase accumulator steps through each of 232 possible outputs before it overflows and restarts. The corresponding output sinewave frequency is equal to the input clock frequency divided by 232. If M=2, then the phase accumulator register "rolls over" twice as fast, and the output frequency is doubled. This can be generalized as follows.



n	Number of Points = 2^n
8	256
12	4,096
16	65,536
20	1,048,576
24	16,777,216
28	268,435,456
32	4,294,967,296
48	281,474,976,710,656

- $10*\log(2^8) = 24dB$
- $10*\log(2^{12}) = 36dB$
- $10*\log(2^{16}) = 48dB$
- $10*\log(2^{20}) = 60dB$
- $10*\log(2^{24}) = 72dB$
- $10*\log(2^{28}) = 84dB$
- $10*\log(2^{32}) = 96dB$
- $10*\log(2^{48}) = 144dB$

Figure 60: Digital Phase Wheel [13]

For an n-bit phase accumulator (n generally ranges from 24 to 32 in most DDS systems), there are 2n possible phase points. The digital word in the delta phase register, M, represents the amount the phase accumulator is incremented each clock cycle. If fc is the clock frequency, then the frequency of the output sinewave is equal to:

$$f_0 = \frac{M \cdot f_c}{2^n} \tag{33}$$

This equation is known as the DDS "tuning equation". Note that the frequency resolution of the system is equal to fc/2n. For n = 32, the resolution is greater than one part in four billion! In a practical DDS system, all the bits out of the phase accumulator are not passed on to the lookup table, but are

truncated, leaving only the first 13 to 15 MSBs. This reduces the size of the lookup table and does not affect the frequency resolution. The phase truncation only adds a small but acceptable amount of phase noise to the final output, (See Figure 61).

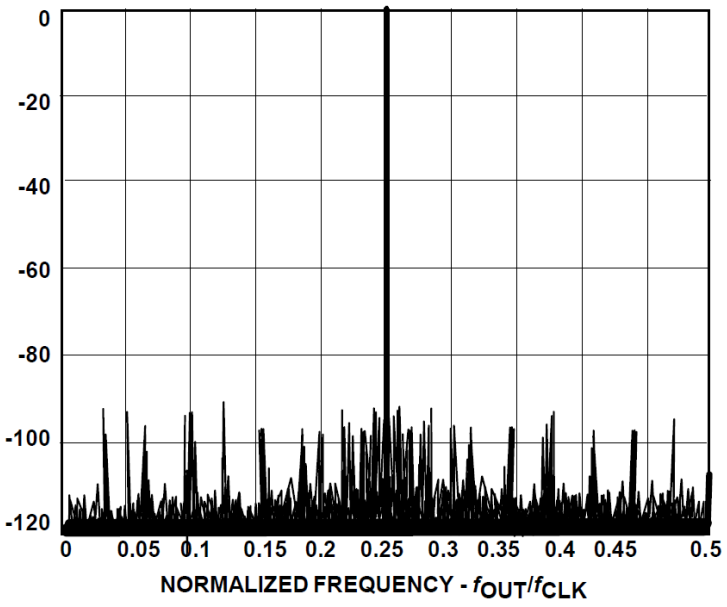


Figure 61: Calculated Output Spectrum Shows 90dB Spurious Free Dynamic Range (SFDR) [13]

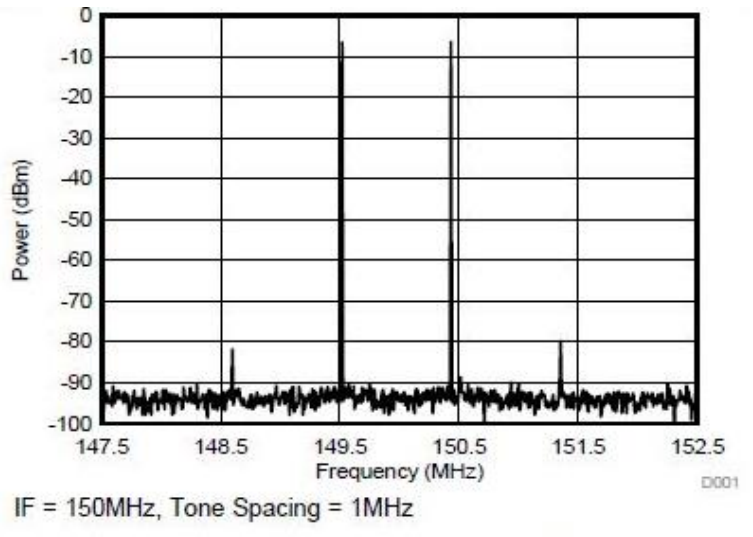


Figure 62: Two-Tone Spectral Plot [13]

The resolution of the DAC is typically 2 to 4 bits less than the width of the lookup table. Even a perfect N-bit DAC will add quantization noise to the output. Figure 61 shows the calculated output spectrum for a 32-bit phase accumulator, 15-bit phase truncation. The value of M was chosen so that the output frequency was slightly offset from 0.25 times the clock frequency. Note that the spurs caused by the phase truncation and the finite DAC resolution are all at least 90 dB below the full-scale output. This performance far exceeds that of any commercially available 12-bit DAC and is adequate for most applications.

The basic DDS system described above is extremely flexible and has high resolution. The frequency can be changed instantaneously with no phase discontinuity by simply changing the contents of the M-register. However, practical DDS systems first require the execution of a serial or byte-loading sequence to get the new frequency word into an internal buffer register which precedes the parallel-output M-register. This is done to minimize package pin count. After the new word is loaded into the buffer register, the parallel-output delta phase register is clocked, thereby changing all the bits simultaneously. The number of clock cycles required to load the delta-phase buffer register determines the maximum rate at which the output frequency can be changed.

ALIASING (Mixing Products) IN DDS SYSTEMS

There is one important limitation to the range of output frequencies that can be generated from the simple DDS system. The Nyquist Criteria states that the clock frequency (sample rate) must be at least twice the output frequency. Practical limitations restrict the actual highest output frequency to about 1/3 the clock frequency. Figure 63 shows the output of a DAC in a DDS system where the output frequency is 30 MHz and the clock frequency is 100 MHz. An antialiasing filter must follow the reconstruction DAC to remove the lower image frequency (100-30=70 MHz) as shown in the figure.

The sampling method is related to a mixer. The frequency to be sampled and the sampling frequency (We distinguish between over and under sampling), reappear as mixing products, following the products like $f_1 \pm f_2$, $2f_1 \pm f_2$, $3f_1 \pm f_2$ or the reverse order, $2f_2 \pm f_1$ etc. aliasing products are the same as mixing products, as mentioned above. The digital community simply resorts to a different nomenclature. The under-sampling of a waveform is sometimes called decimation. E.g. – if we sample different points of ten consecutive identical waveforms, the number of points to reconstruct is reduced by a factor of 10. This reduces the memory requirement and the computational power, but it does not ultimately improve the S/N ratio.

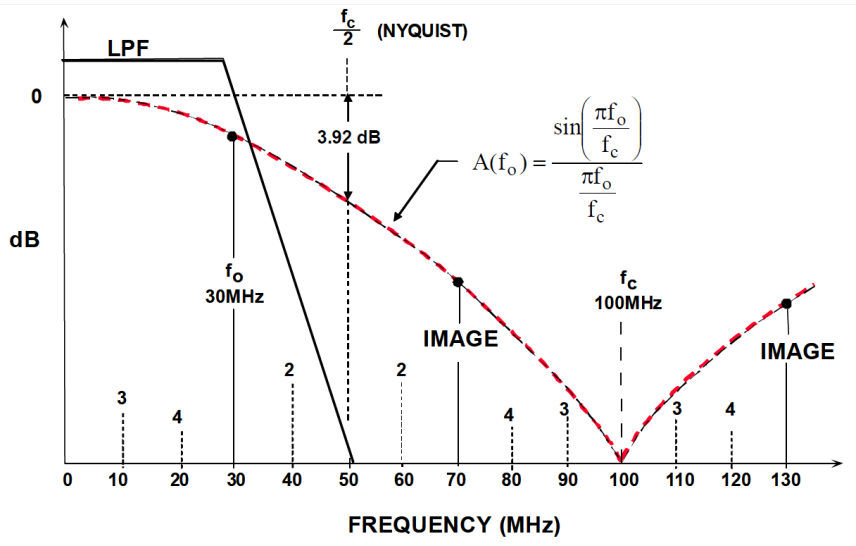


Figure 63: Aliasing in a DDS System [13]

Note that the amplitude response of the DAC output (before filtering) follows a sin(x)/x response with zeros at the clock frequency and multiples thereof. The exact equation for the normalized output amplitude, $A(f_0)$ is given by:

$$A(f0) = \frac{\sin\left(\frac{\pi f_0}{f_c}\right)}{\frac{\pi f_0}{f_c}} \quad (34)$$

Where f_0 is the output frequency and f_c is the clock frequency.

This rolloff is because the DAC output is not a series of zero-width impulses (as in a perfect re-sampler), but a series of rectangular pulses whose width is equal to the reciprocal of the update rate. The amplitude of the sin(x)/x response is down 3.92 dB at the Nyquist frequency (1/2 the DAC update rate). In practice, the transfer function of the antialiasing filter can be designed to compensate for the sin(x)/x rolloff so that the overall frequency response is relatively flat up to the maximum output DAC frequency (generally 1/3 the updated rate).

Another important consideration is that, unlike a PLL-based system, the higher order harmonics of the fundamental output frequency in a DDS system will fold back into the baseband because of aliasing. These harmonics cannot be removed by the antialiasing filter. For instance, if the clock frequency is 100 MHz, and the output frequency is 30 MHz, the second harmonic of the30 MHz output signal appears at 60 MHz (out of band), but also at 100 – 60 = 40 MHz (the aliased component. Similarly, the third harmonic (90 MHz) appears inband at 100 – 90 = 10MHz, and the fourth at 120 – 100 MHz = 20 MHz. Higher order harmonics also fall within the Nyquist bandwidth (dc to $f_c/2$). The location of the first four harmonics is shown in the figure.

Modern digital techniques allow high order filter to be designed, to clean up the output down to -100dB.

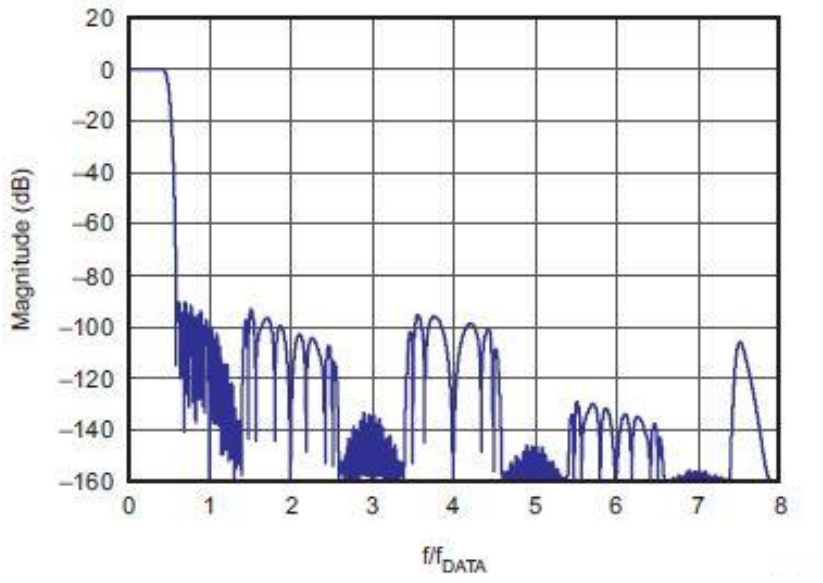


Figure 64: Composite Frequency Response of a High-Order Clean-Up Filter [14]

Amplitude modulation in a DDS system

Amplitude modulation in a DDS system can be accomplished by placing a digital multiplier between the lookup table and the DAC input as shown in Figure 65. Another method to modulate the DAC output amplitude is to vary the reference voltage to the DAC. In the case of the AD9850, the bandwidth of the

internal reference control amplifier is approximately 1MHz. This method is useful for relatively small amplitude changes as long as the output signal does not exceed the +1V compliance specification.

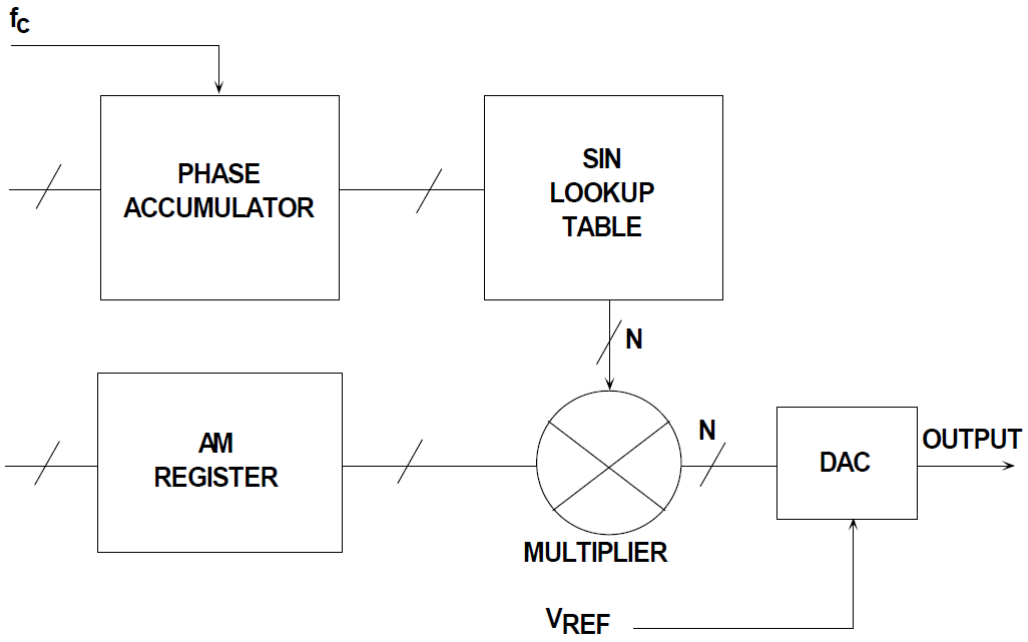


Figure 65: Amplitude Modulation in a DDS System

Different Waveforms:

These modern DDS systems like the 9911-9914 series have some hard-wired signals which are used for cellular telephones as an example. The architecture shown above is flexible enough to generate in the true sense, arbitrary waveforms. In addition to this, mathematical tools can generate the necessary entries to lookup tables, not only for sine and cosine values, but truly determine any mathematical functions.

SPURIOUS FREE DYNAMIC RANGE CONSIDERATIONS IN DDS SYSTEMS

In many DDS applications, the spectral purity of a DAC output is of primary concern. Unfortunately, the measurement prediction and analysis of this performance is complicated by a number of interacting factors.

Even an ideal N-bit DAC will produce harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of the output frequency to the clock frequency. This is because the spectral content of the DAC quantization noise varies as this ratio varies, even though its theoretical rms value remains equal to q/√12 (where q is the weight of the LSB). The assumption that the quantization noise appears as white noise and is spread uniformly over the Nyquist bandwidth is simply not true in a DDS system (it is more apt to be a true assumption in an ADC-based system, because the ADC adds a certain amount of noise to the signal which tends to "dither" or randomize the quantization error. However, a certain amount of correlation still exists). For instance, if the DAC output frequency is set to an exact submultiple of the clock frequency, then the quantization noise will be concentrated at multiples of the output frequency, i.e., it is highly dependent. If the output frequency is slightly offset,

however, the quantization noise will become more random, thereby giving an improvement in the effective SFDR.

This is illustrated in Figure 66, where a 4096 (4k) point FFT is calculated based on digitally generated data from an ideal 12-bit DAC. In the left-hand diagram (A), the ratio between the clock frequency and the output frequency was chosen to be exactly 40, yielding an SFDR of about 77dBc. In the right-hand diagram, the ratio was slightly offset, and the effective SFDR is now increased to 94 dBc. In this ideal case, we observed a change in SFDR of 17 dB just by slightly changing the frequency ratio.

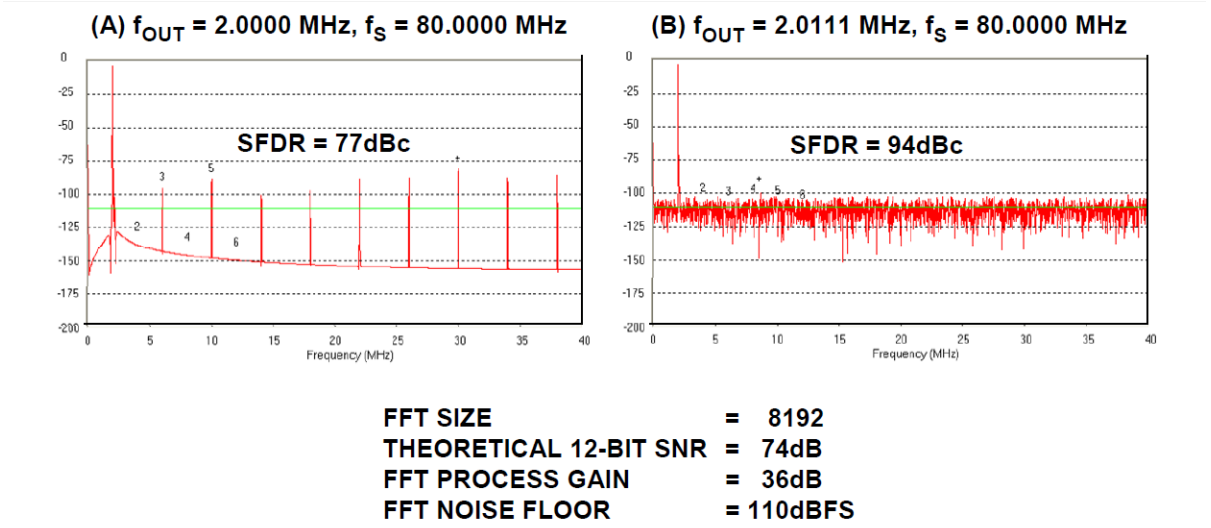


Figure 66: Effect of Radio of Clock to Output Frequency on Theoretical 12-bit DAC SFDR using 4096 Point FFT [13]

Best SFDR can therefore be obtained by the careful selection of the clock and output frequencies. However, in some applications, this may not be possible. In ADC-based systems, adding a small amount of random noise to the input tends to randomize the quantization errors and reduce this effect. The same thing can be done in a DDS system as shown in Figure 67 (See References 8, 9, 10). The pseudo-random digital noise generator output is added to the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about 1/2LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor. In most DDS applications, however, there is enough flexibility in selecting the various frequency ratios so that dithering is not required.

A particular interesting integrated circuit from Analog Devices is AD9911. The following is a brief summary of its capability.

GENERAL DESCRIPTION

The AD9911 is a complete direct digital synthesizer (DDS). This device includes a high speed DAC with excellent wideband and narrowband spurious-free dynamic range (SFDR) as well as three auxiliary DDS cores without assigned digital-to-analog converters (DACs). These auxiliary channels are used for spur reduction, multitone generation, or test-tone modulation.

The AD9911 is the first DDS to incorporate SpurKiller technology and multitone generation capability. Multitone mode enables the generation up to four concurrent carriers; frequency, phase and amplitude can be independently programmed. Multitone generation can be used for system tests, such as inter-modulation distortion and receiver blocker sensitivity. SpurKilling enables customers to improve SFDR

performance by reducing the magnitude of harmonic components and/or the aliases of those harmonic components.

Test-tone modulation efficiently enables sine wave modulation of amplitude on the output signal using one of the auxiliary DDS cores.

The AD9911 can perform modulation of frequency, phase, or amplitude (FSK, PSK, ASK). Modulation is implemented by storing profiles in the register bank and applying data to the profile pins. In addition, the AD9911 supports linear sweep of frequency, phase, or amplitude for applications such as radar and instrumentation.

This hard-wired capability makes the AD9911 very useful in signal generators, as all the coefficients are already stored and do not need to be calculated.

The following block diagram shows the very powerful AD9914, which is used for much higher frequencies.

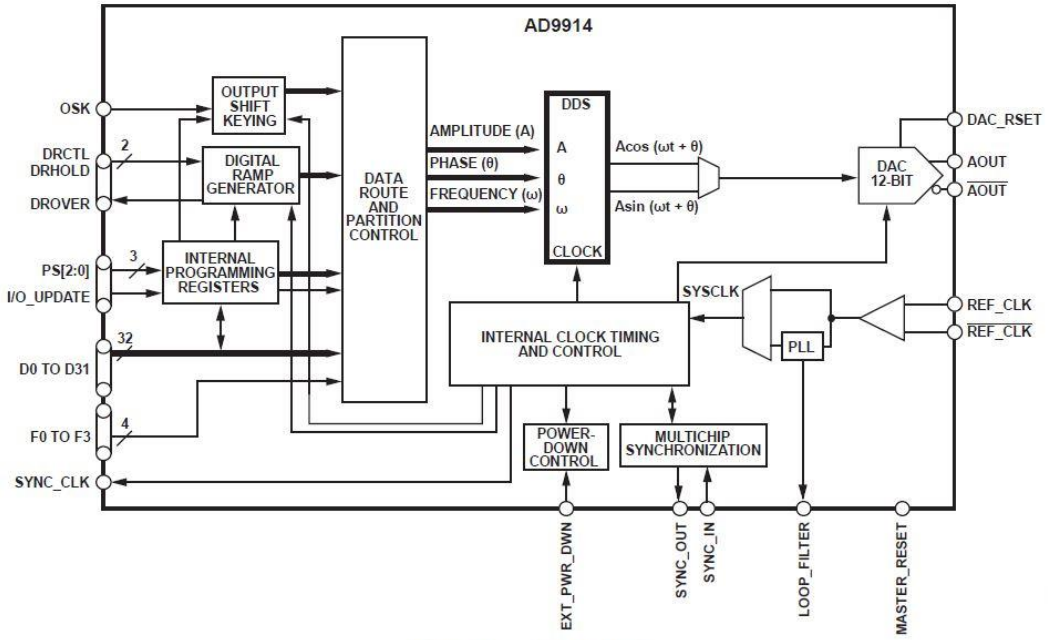


Figure 2. Detailed Block Diagram

Figure 67: Detailed Block Diagram of the AD9914 [12]

The detailed block diagram of the AD9914 requires some comments. The desired output frequency is delivered from the 12-bit DAC where 2^{12}=4096, is the resolution. The actual frequency is generated in the DDS portion on the left. It mentions Sine and Cosine functions. However the entire left block can be setup to generate arbitrary waveforms.

As to the clock generation, which should be as high as possible, but not higher than 3.5GHz, the built-in PLL on the lower right side of the block diagram, labeled as REF_CLK can be used to generate such a frequency. However, much better performance is obtained from a ultra-stable clock synthesizer, like the R&S SMA100B.

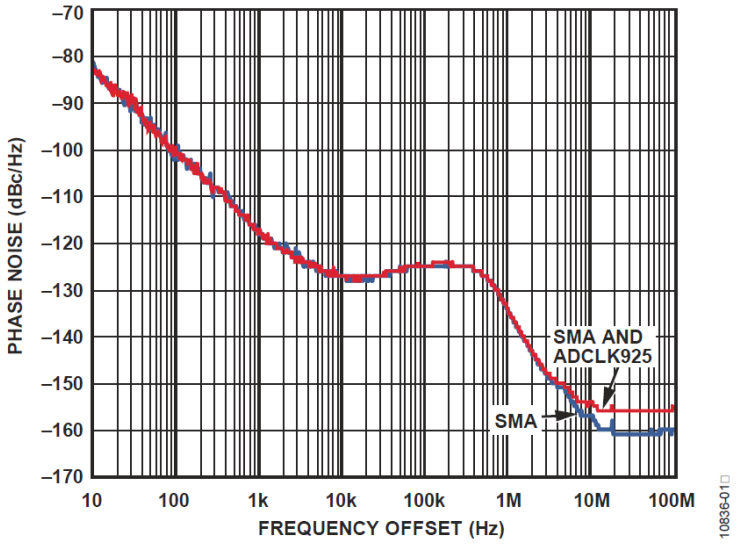


Figure 68: Absolute Phase Noise of REF CLK Source Driving AD9914 Rohde and Schwarz SMA100 Signal Generator at 3.5GHz Buffered by Series ADCLK925 [12]

Phase Noise in DDS (Figure 69 to Figure 73 - Courtesy and Permission - Prof. Enrico Rubiola)

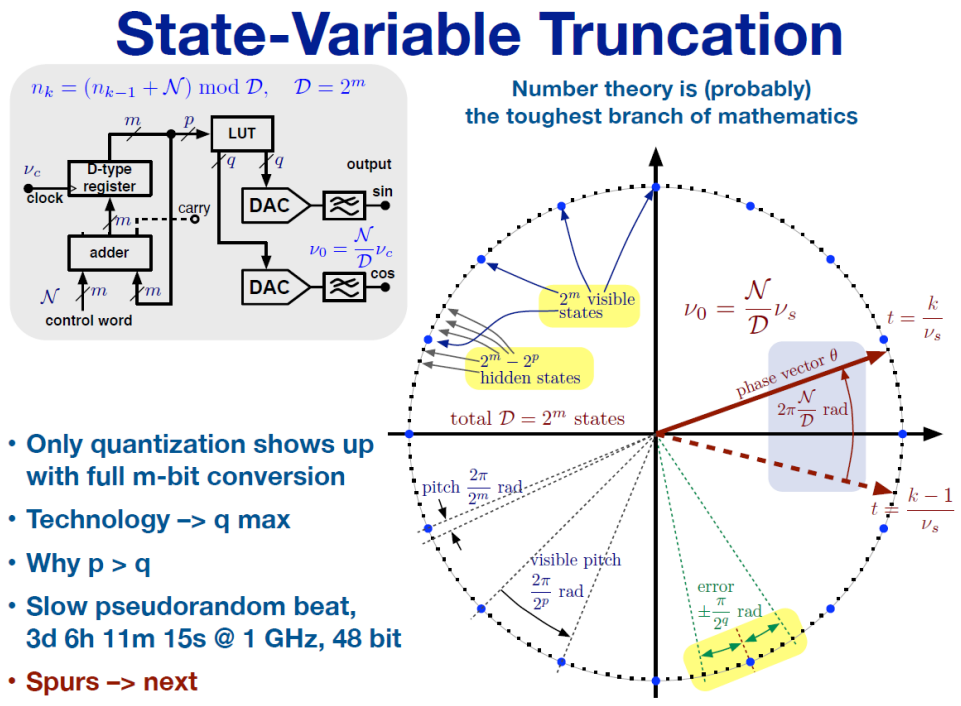


Figure 69: State Variable Truncation

Nonlinearity Generates Spurs

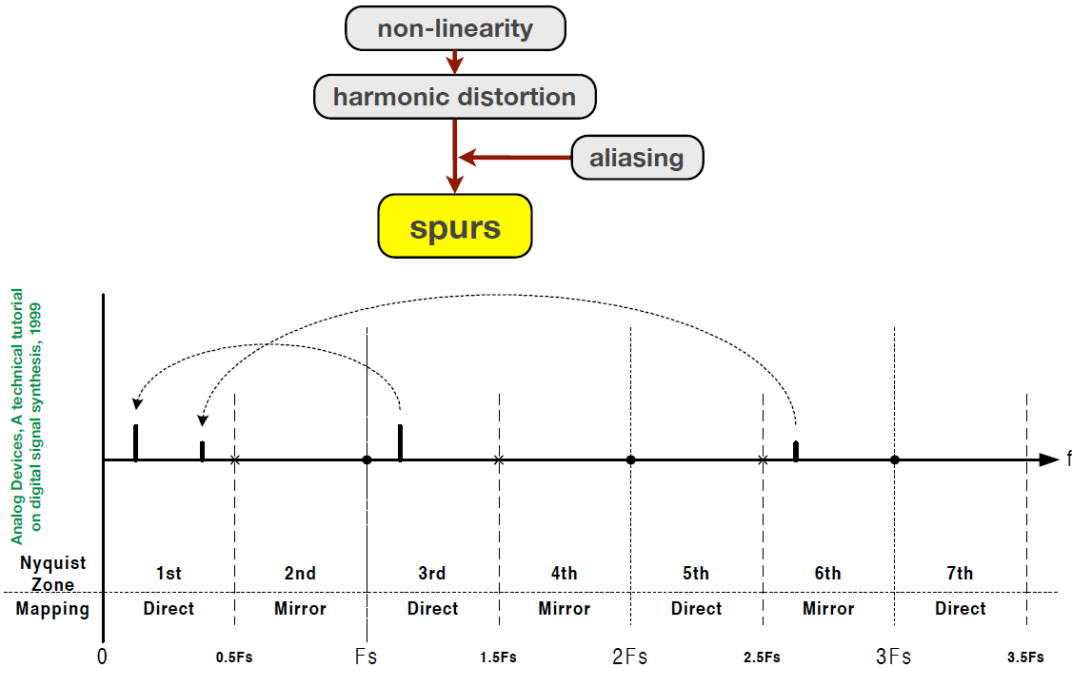


Figure 70: Nonlinearity Generates Spurs

Spurs Can Swallow Noise

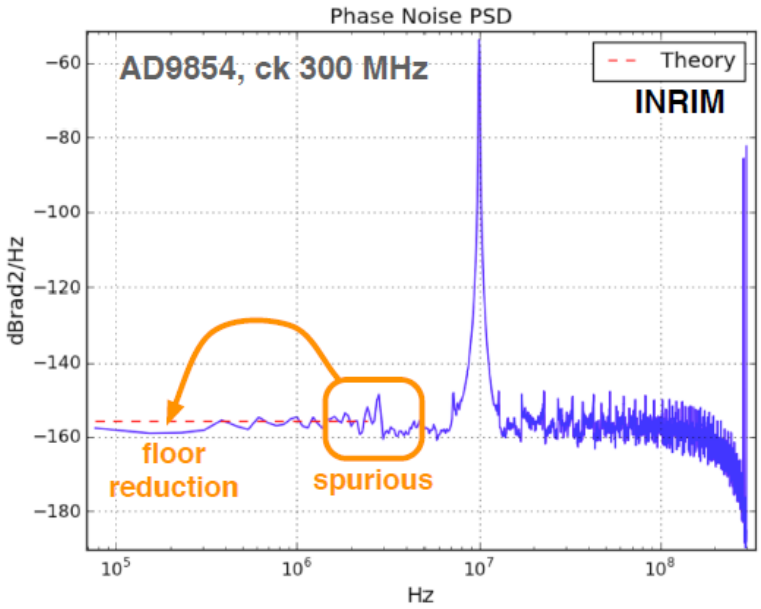
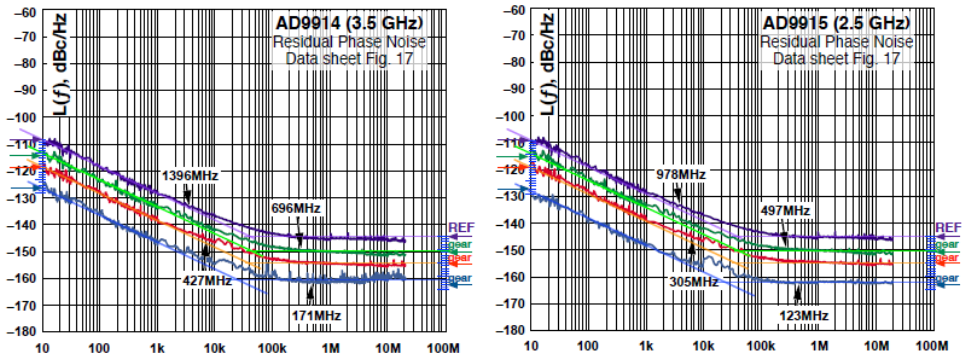


Figure 71: Spurs Can Swallow Noise

High-Frequency DDSs

AD9914 12 bit, 3.5 GHz
64 bit accumulator (190 pHz res)

AD9915 12 bit, 2.5 GHz
64 bit accumulator (135 pHz res)



Residual noise is close to that of the gear-box model

Plots are from the manufacturer data sheet

Whether spurs are removed or not, is not said

Figure 72: High-Frequency DDS

AD9854 I-Q Noise

Flicker is in quite a good agreement between YG and CC

I–Q spectra cannot be compared to specs

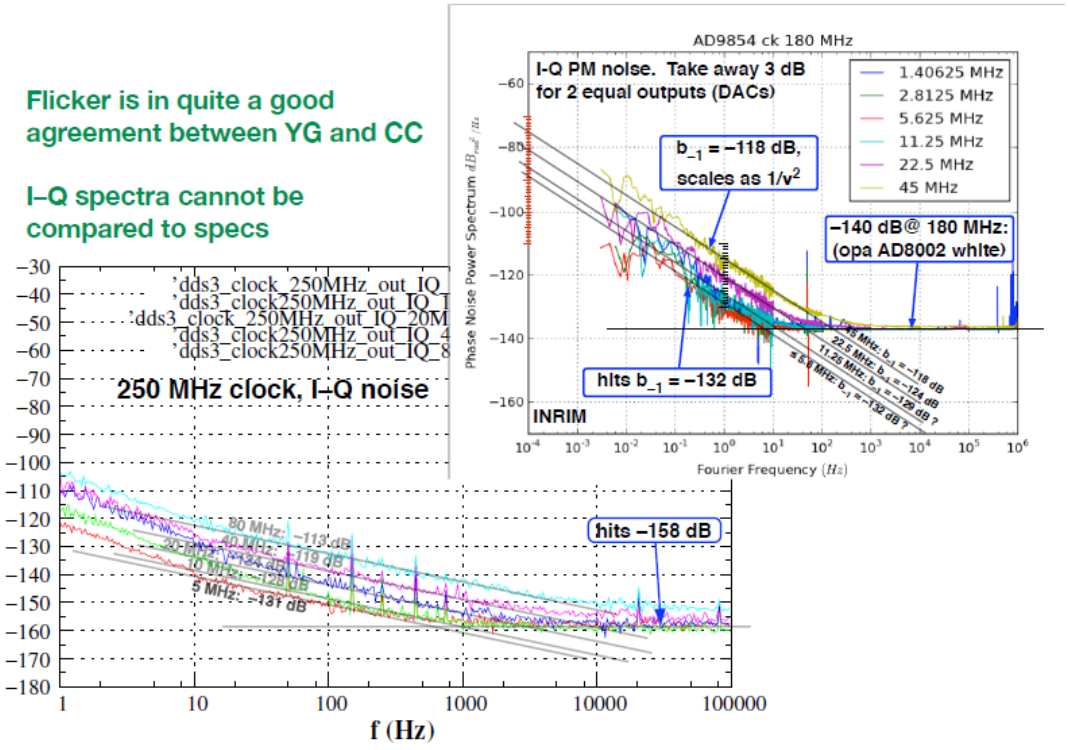


Figure 73: AD9854 I-Q Noise

Arbitrary Waveform Generation with Interpolation (Under-sampling):

The restrictions of the Nyquist limit are well known. In order to avoid aliasing (overlapping of spectra), the minimum sampling frequency f_s must be equal to or greater than twice the highest frequency of interest f_g. See Figure 74.

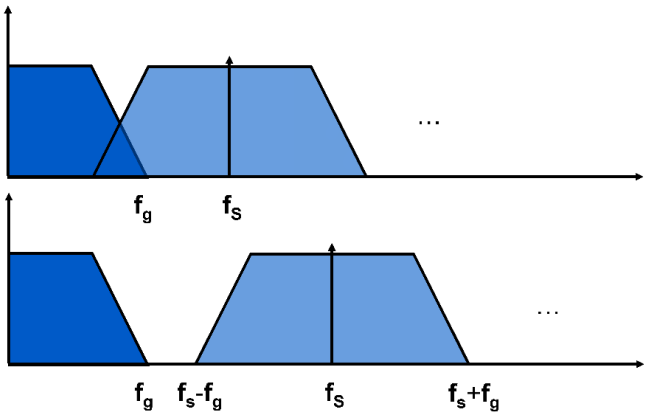


Figure 74: Nyquist relationships. (From [6] Used with permission)

A reconstruction filter is used for suppression of aliasing products. To achieve adequate suppression, in general, only about 80% of the Nyquist bandwidth can be used, as illustrated in Figure 75.

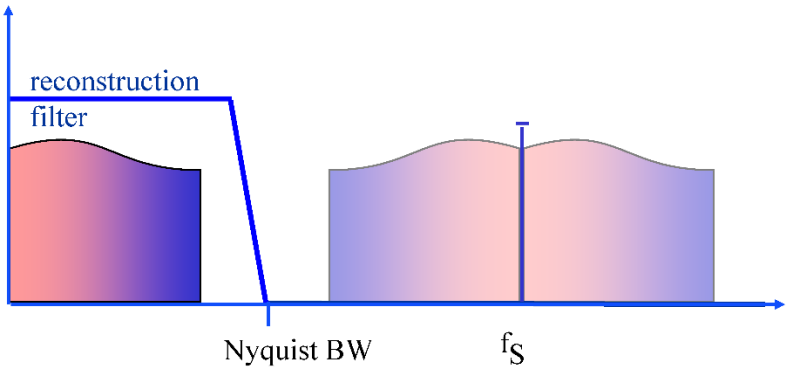


Figure 75: Influence of a reconstruction filter on the Nyquist bandwidth. (From [6] Used with permission)

The system consists of three major stages:

- Output memory containing the desired wave form (either in data points or mathematical expressions)
- D/A converter
- Analog low pass filter

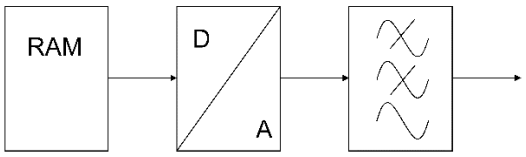


Figure 76: Simplified block diagram of an arbitrary waveform generator. (From [6] Used with permission)

Due to the limited number of filters and their steepness, the sampling rate often has to be set considerably higher than required by Nyquist's theorem in order for the aliasing effects to be sufficiently suppressed by the analog filter.

In Figure 78, the leftmost trace of the frequency domain illustrates a 1 MHz sinewave signal and the mirror frequencies around the sampling frequency of 12 MHz. In the following D/A conversion, the discrete impulses are transformed into an analog waveform. Because a voltage level is present for the time 1/(clock rate of the D/A converter) a waveform results that is built out of single rectangles. Fourier-transformed rectangles result in a sin(*x*)/*x*-function in the frequency domain. Therefore, the D/A conversion is weighting the signal with a sin(*x*)/*x*-function.

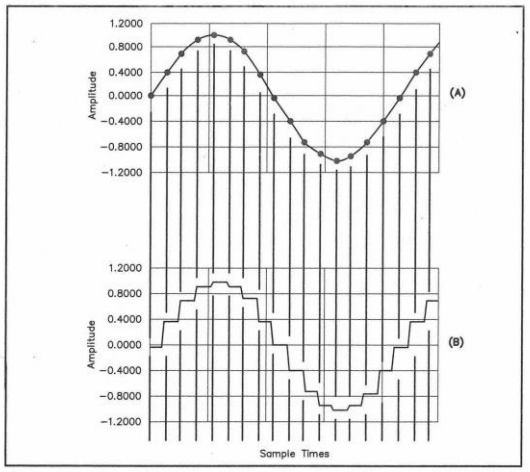


Figure 77: Oversampling of a Sine Wave(From [6] Used with permission)

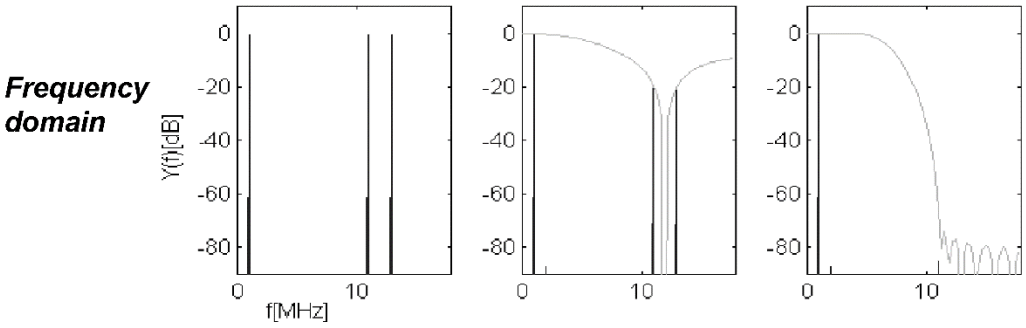


Figure 78: Principal waveforms of a conventional arbitrary waveform generator. (From [6] Used with permission)

If we have a 1 MHz sine wave and a filter with a cut off frequency of 11 MHz, a sampling rate of at least 12 MHz must be selected to make sure that the aliasing effects are sufficiently suppressed (Figure 79). Due to sampling with the sampling frequency f_s = 12 MHz, we can see the 1 MHz (baseband) sine wave at 13 MHz and as mirror at 11 MHz.

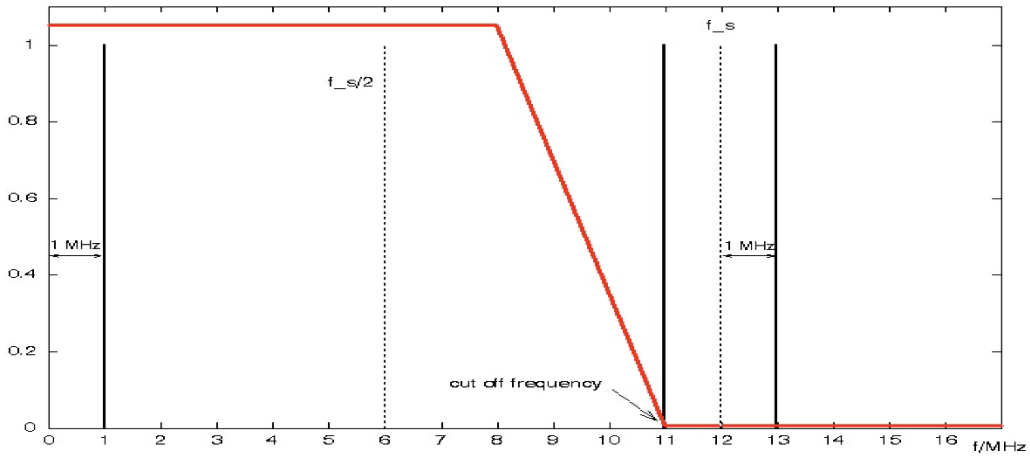


Figure 79: Effect of sampling rate and filtering on cutoff frequency. (From [6] Used with permission)

A modern arbitrary waveform generator, illustrated in Figure 80, substantially consists of:

- Output memory (can be configured, does NOT have to be a sinusoidal waveform!)
- An interpolation filter
- D/A converter
- Analog low pass filter

The waveform stored in the non-volatile memory of the system is interpolated to a higher sampling rate by means of a very steep-edged, digital interpolation filter before it is output. The interpolation rate of the digital filter may be automatically set such that aliasing of the interpolated sampling rate is suppressed by the analog filter. The memory needed to store the waveform can be much shorter (smaller) than in a conventional arbitrary waveform generator because of the lower original sampling rate.

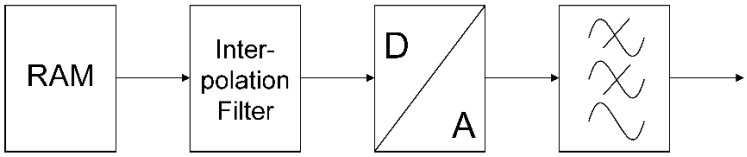


Figure 80: Simplified block diagram of a modern arbitrary waveform generator. (From [6] Used with permission)

The function principle is shown in Figure 81 for a 1 MHz sine wave signal. In the leftmost trace of the frequency domain, the 1 MHz sinewave and the mirrors resulting from the sampling rate of 3 MHz are shown. The following digital interpolation filter suppresses unwanted aliasing (mixing) products. This gives a higher sampling rate and therefore, as shown in the second trace, more values in the time

domain. The D/A conversion is weighting the signal with a sin(*x*)/*x*-function. The analog filter suppresses the aliasing components of that signal.

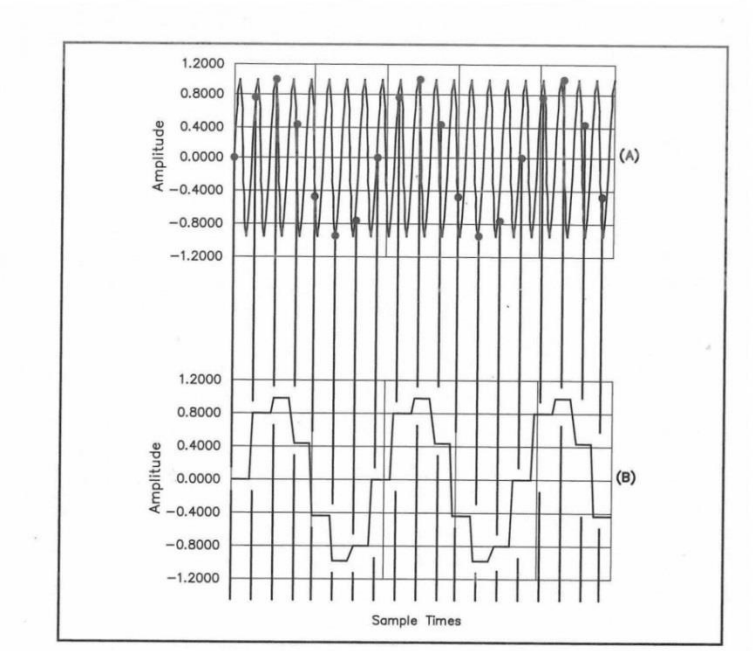


Figure 81: Effect of Under-Sampling (From [6] Used with permission)

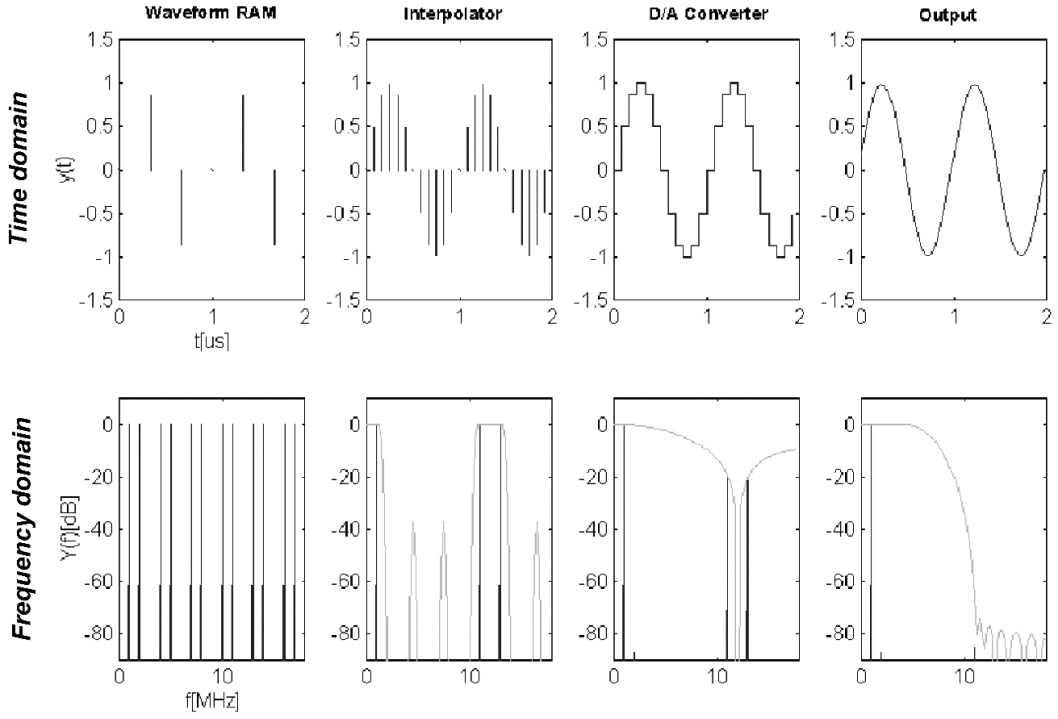


Figure 82: Principal waveforms of a modern arbitrary waveform generator. (From [6] Used with permission)

An example 1 MHz sine wave signal is shown in Figure 83. The waveform is sampled with a 12 MHz sampling rate, which means that every 83.3 ns one value is taken. The resulting frequency domain is displayed. Here we have the 1 MHz original signal (in baseband) and the aliasing product (mixing or spurious products) of the original signal at multiples of the sampling frequency (12 MHz, 24 MHz, 36 MHz, and so on, but only 12 MHz is shown).

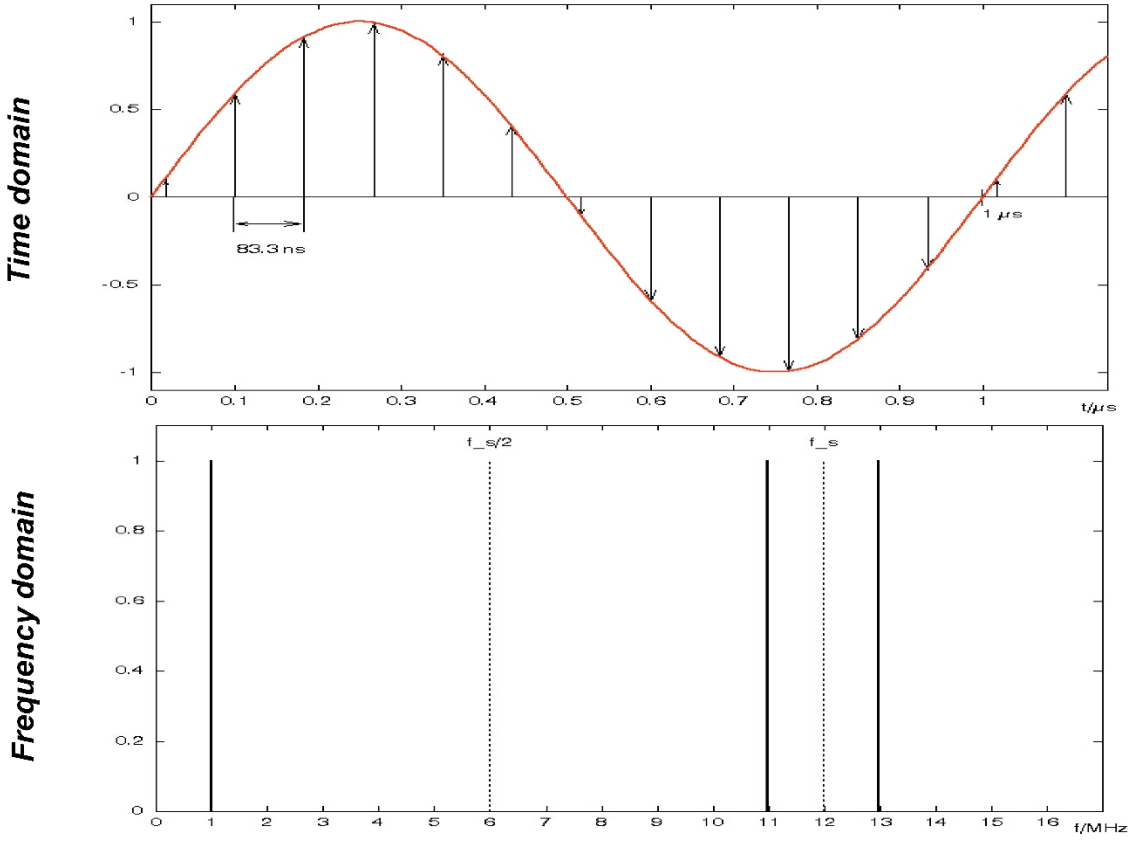


Figure 83: Example of interpolation in a modern arbitrary waveform generator. Shown is a 1 MHz sine wave with a 12 MHz sampling frequency. (From [6] Used with permission*)*

Figure 84 shows the same 1 MHz sine wave signal, but this time it is sampled at a rate of 3 MHz, which means that every 333 ns one value is taken. This results in the spectrum trace shown. It can be seen that we have the 1 MHz original signal and aliasing products at every sampling rate multiple.

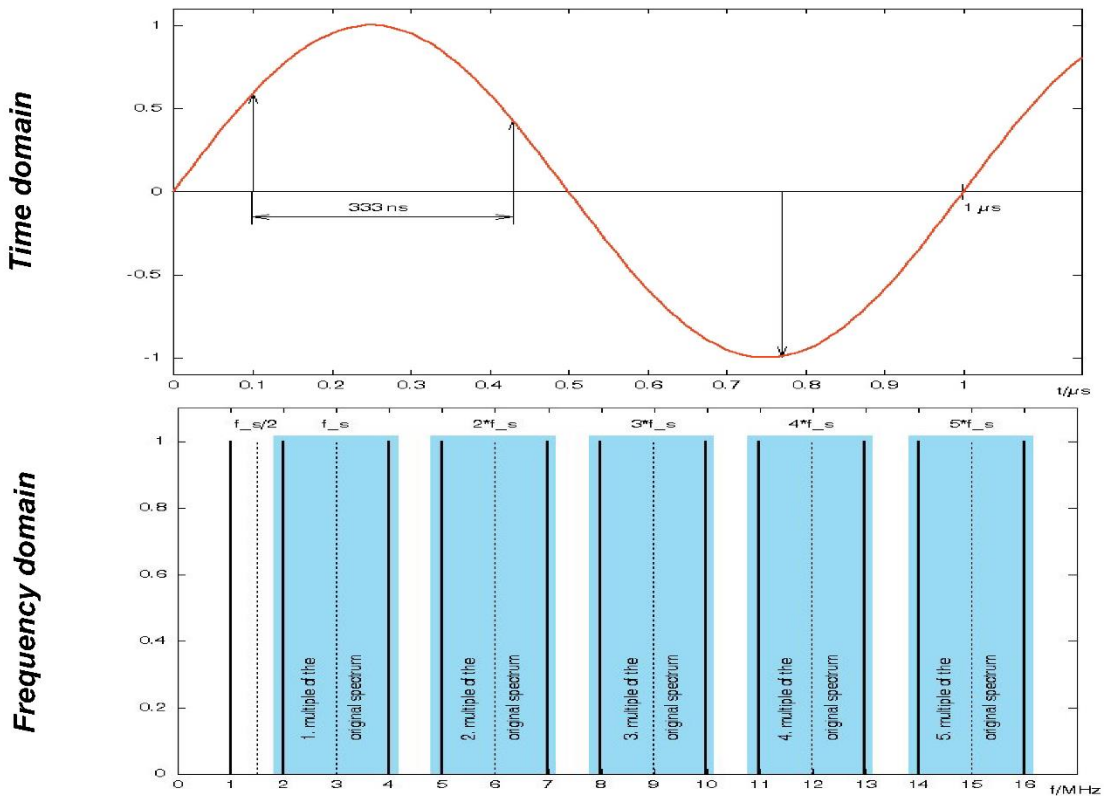


Figure 84: Example of interpolation in a modern arbitrary waveform generator. Shown is a 1 MHz sine wave with a 3 MHz sampling frequency. (From [6] Used with permission)

By applying the digital interpolation filter, all unwanted aliasing products are suppressed, as shown in Figure 85. In this example, only the frequencies within the red area pass the filter, which means that the filter provides an oversampling of 4 (3 MHz × 4 = 12 MHz). As result, we have exactly the same frequency display as for a 12 MHz sampling rate.

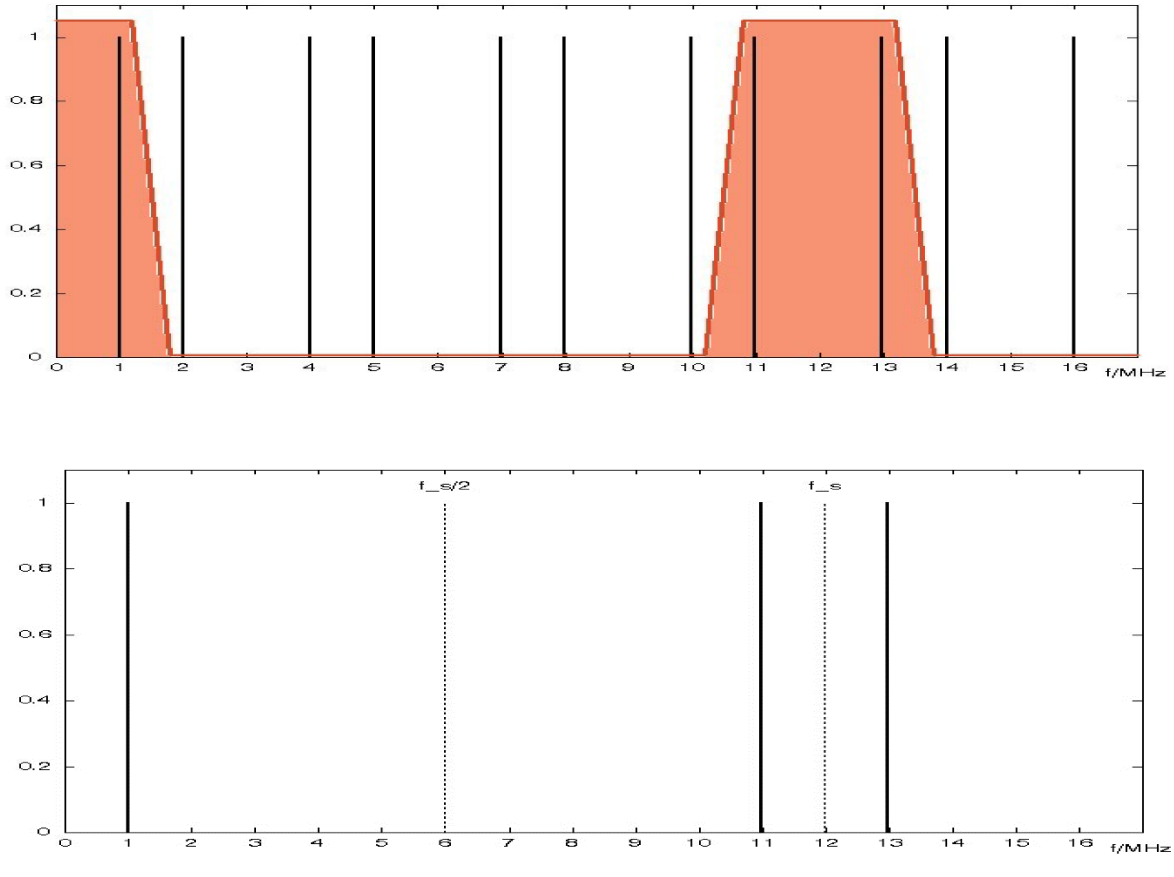


Figure 85: Analysis of the interpolation example of Figure 84: (*a*) 1 MHz sine wave with a 3 MHz sampling rate, (*b*) after interpolation. (From [6] Used with permission)

By use of interpolation, waveforms can be sampled with a lower sampling rate, which means a lower amount of memory necessary to store the waveform. This results in less memory, required within the signal generator and a more efficient overall system [6].

About Bits, Symbols and Waveforms [1]

Introduction

Digital modulation of an RF carrier is the allocation of physically existing RF waveforms to the single elements of an alphabet of logical symbols where the number of allowed waveforms is equal to the number of logical elements of the alphabet (Figure 86). The most common alphabet is the binary one with the 2 logical symbols "0" and "1", but we will also deal with quaternary, octernary and hexadecimal alphabets or more generally with *M*-ary alphabets comprising many more elements when discussing the signal generation with signal generators and dedicated software packages. The waveforms representing these symbols differ from each other by their parameters amplitude a(t), their frequency f(t) and their phase $\varphi(t)$.

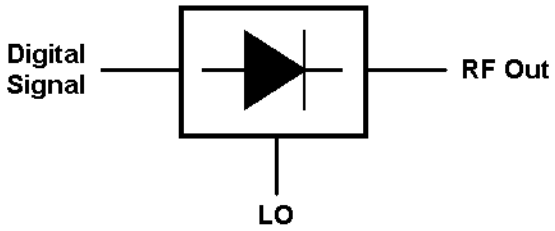


Figure 86: At base, digital modulation involves frequency-shifting a baseband digital signal to RF. In practice, the process is more complicated than this because of bandwidth constraints on the resulting RF signal [1]

A modulator therefore is nothing more than a device by which this allocation is performed (Figure 87). From a coder it receives the logical symbols and emits at its output the corresponding waveforms $s_i(t)$. The waveform generation may be done by using a set of distinct generators (for example, two oscillators to generate two signals with different frequencies in the case of binary frequency shift keying), by classical amplitude or frequency modulators or by more sophisticated equipment such as I/Q-modulators for *M*-ary modulations.

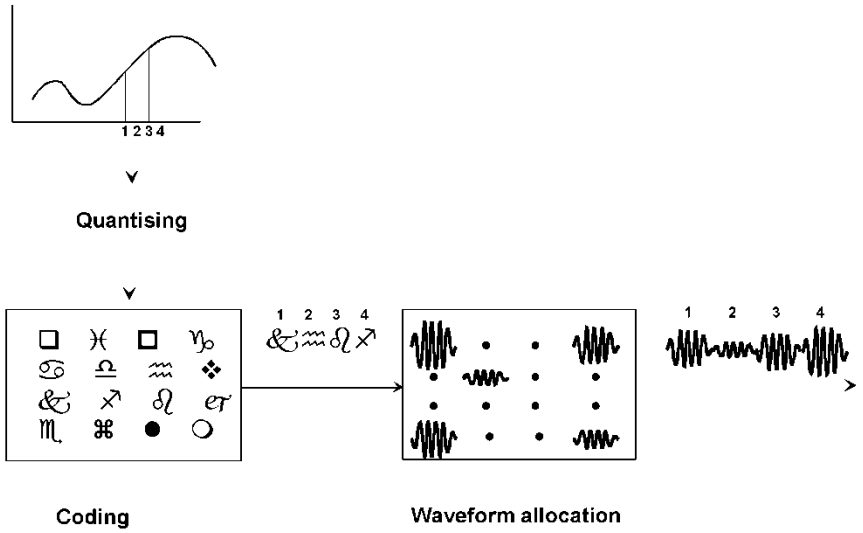


Figure 87: Digital modulator [1]

On their way across the RF channel from the transmitter to the receiver, these waveforms are distorted by noise and other disturbing properties of the RF channel.

The task of the receiver is to interpret the received waveforms $r_i(t)$ and to reallocate the proper logical symbols to them. For this purpose it is not necessary to reconstruct the original waveforms from the distorted ones (Figure 88). The important thing is to find out which symbol has most probably been sent when a certain signal $r_i(t)$ has been received, a process which is known as maximum likelihood estimation.

For meaningful receiver tests therefore waveforms have to be generated that mimic real, distorted signals to prove the ability of a receiver to tolerate waveform distortions to a certain extent.

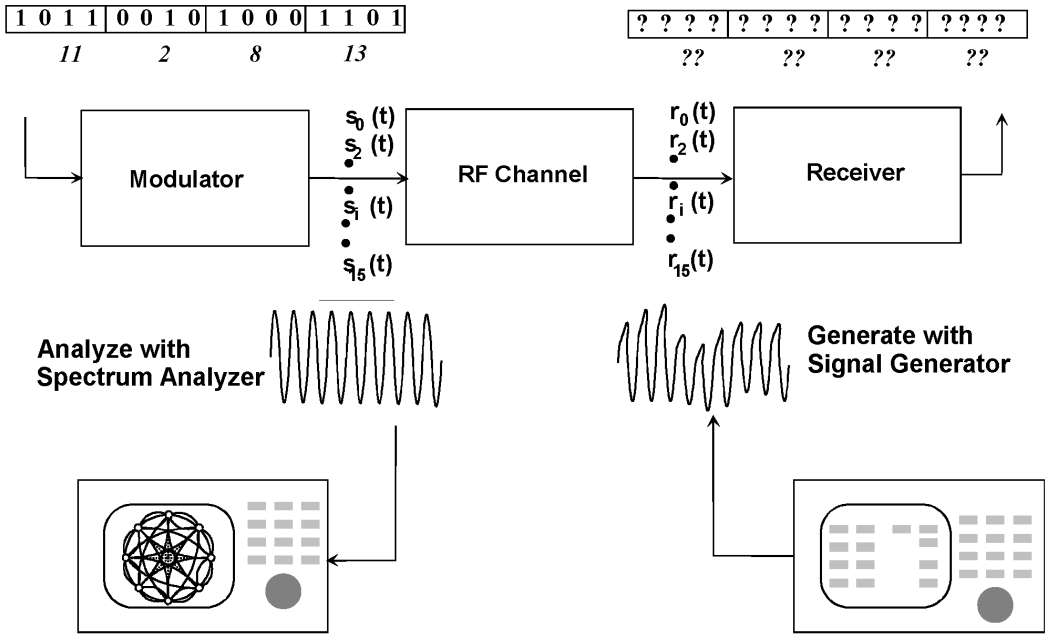


Figure 88: The information channel [1]

Representation of a Modulated RF Carrier: The waveform of a modulated RF-carrier can be expressed as

$$s(t) = a(t)\cos\left[2\pi f_c(t)t + \varphi(t)\right] \tag{35}$$

and is defined by its amplitude $a(t)$, its carrier frequency $f_c(t)$ and its phase $\varphi(t)$. All the three parameters are time variant and may be altered to generate different waveforms to represent logical symbols. If the occupied bandwidth of this modulated carrier is narrow, compared to the carrier frequency f_c, we call this signal the *RF-bandpass signal* (Figure 89)**.**

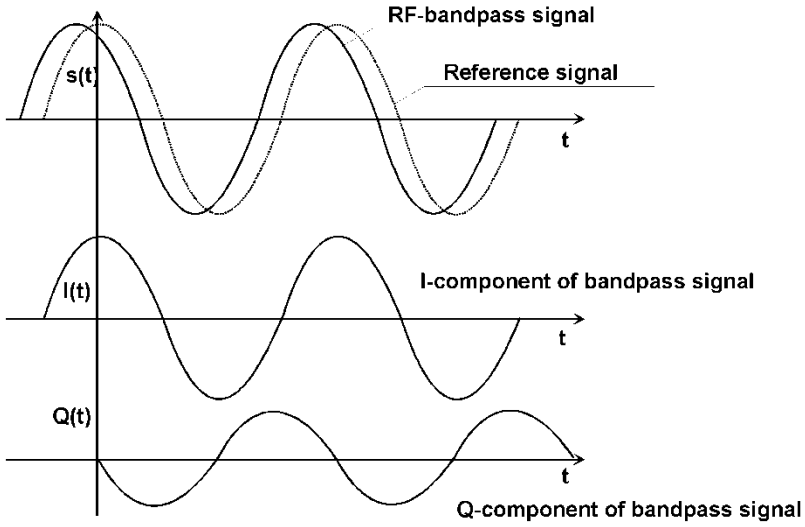


Figure 89: The bandpass signal and the I/Q representation of a carrier [1]

As any frequency variation causes a phase variation and vice versa a phase variation always causes a frequency variation, we can replace any frequency modulation by a corresponding phase modulation. Therefore we simplify the above equation to

$$s(t) = a(t)\cos\left[2\pi f_c t + \varphi(t)\right] \tag{36}$$

that is, we consider the carrier frequency as a constant and concentrate all frequency and phase variations into the parameter $\varphi(t)$.

For our purposes another representation is more suitable, we'll have to look up some trigonometric identities and our formula processor finds that

$$\begin{aligned} a(t)\cos\left[2\pi f_c t + \varphi(t)\right] = {} & \cos\left[\varphi(t)\right] a(t)\cos(2\pi f_c t) \\ & - \sin\left[\varphi(t)\right] a(t)\sin(2\pi f_c t) \end{aligned} \tag{37}$$

which we call the *I/Q* representation of the RF-signal. I/Q means that we have an I (in phase) signal, namely, $\cos\left[\varphi(t)\right]a(t)\cos(2\pi f_c t)$, and a Q (quadrature) signal, namely $-\sin\left[\varphi(t)\right]a(t)\sin(2\pi f_c t)$. These equations help us a lot in understanding an I/Q modulator. Because of the phase difference of 90° between the two carrier components, these are said to be orthogonal to each other.

All the information about the (modulated) carrier with the carrier frequency f_c is contained in the terms

$$c_I(t) = a(t)\cos\left[\varphi(t)\right] \tag{38}$$

$$c_Q(t) = a(t)\sin\left[\varphi(t)\right] \tag{39}$$

and, lazy as we are, we therefore disregard the terms $\cos(2\pi f_c t)$ and $-\sin(2\pi f_c t)$ for further considerations and denote the above signals $c_I(t)$ and $c_Q(t)$ as the components of the *complex baseband waveform* or *baseband signal*.

This leads us immediately to the *vector representation* of the signal, where we consider the two components $c_I(t)$ and $c_Q(t)$ of the complex baseband signal as the time-variant components of a time variant vector with the vector length $a(t)$ and the angle to the I-axis $\varphi(t)$.We also get

$$a(t) = \sqrt{c_I^2(t) + c_Q^2(t)} \tag{40}$$

$$\varphi(t) = \arctan\left(\frac{c_Q}{c_I}\right) \tag{41}$$

The vector can be depicted in the I/Q area (Figure 90).

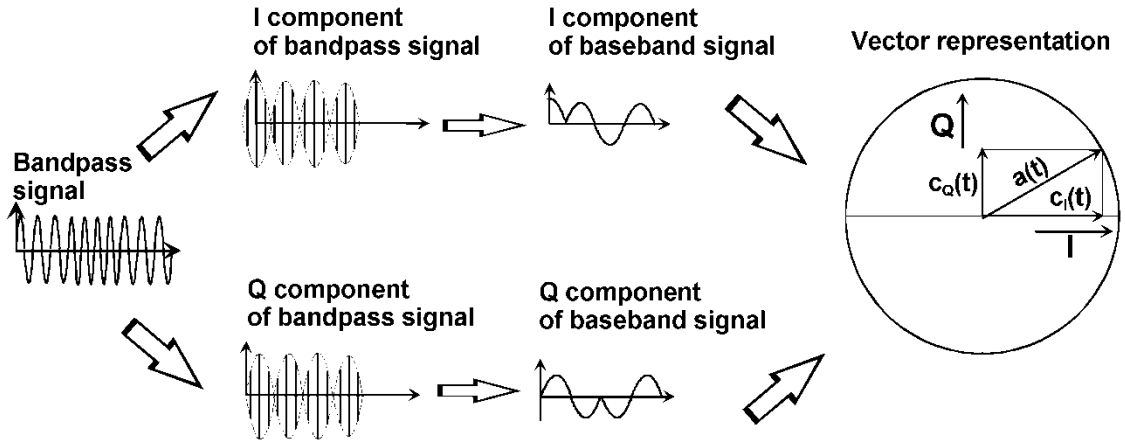


Figure 90: Different forms of signal representation [1]

Generation of the Modulated Carrier:

Once we have realized that the modulated carrier can be represented as the sum of it's I and Q components, which are the product of the two baseband components with two orthogonal RF-carriers of the same frequency, it is easy to understand the hardware of the modulator (Figure 91). An unmodulated RF carrier is split up into two equal oscillations $\cos(2\pi ft)$, one of the two is then shifted by 0.5π, and therefore is described by $-\sin(2\pi ft)$. The component $\cos(2\pi ft)$ is multiplied with the I component of the baseband signal $c_I(t)$, the other one, $-\sin(2\pi ft)$, is multiplied with the Q component $c_Q(t)$ of the baseband signal. Each multiplication may be performed using a double-balanced mixer. Afterwards the two RF-components are added in a simple power combiner. As it is difficult to shift the carrier by 90° over a broad frequency range, the modulated carrier is generated at an intermediate frequency and then upconverted to the wanted output frequency in a second mixer stage.

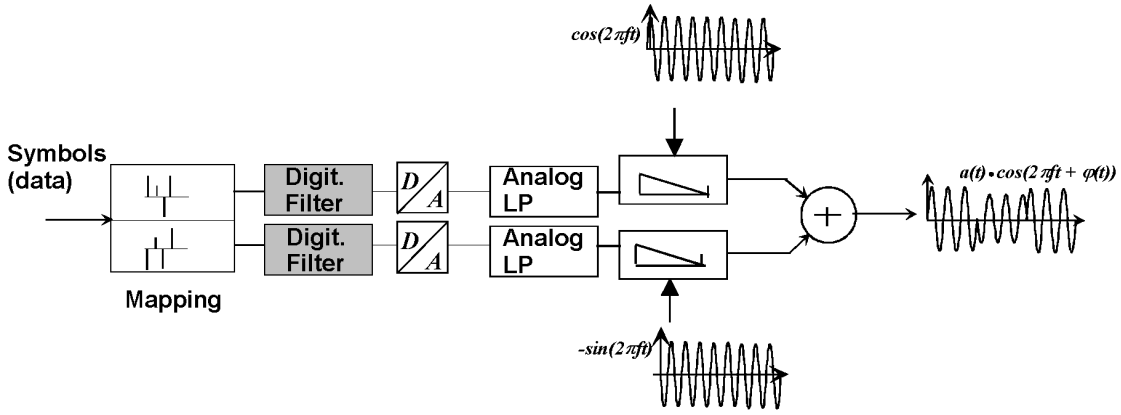


Figure 91: Principle of a digital I/Q modulator [1]

The baseband signals are generated by mapping every digital symbol into a pair of digital pulses which are fed to digital baseband filters. The output signal of these filters is D/A converted and smoothened by analog low-pass filters.

Figure 92 shows another example where, for a given modulation (MSK or GMSK), the instantaneous phase and then the corresponding co-sinusoid and sinusoid, that modulates the two carrier components, is calculated from the data signal.

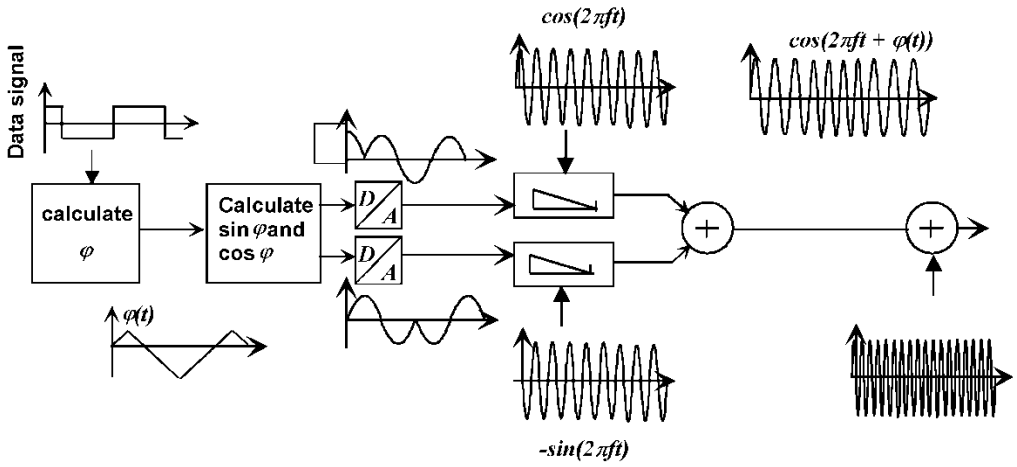


Figure 92: I/Q modulation (MSK and GMSK) [1]

Digital designs of the modulator also exist, in which the IF-carrier generation, the time-variant phase shift, the multiplication with the baseband signals, and the sum of the components are calculated in a digital signal processor, the output of which is D/A-converted and upconverted to the output frequency

in the classical way. A further possibility is the generation of the modulated carrier with direct digital synthesis (DDS), as it is used in the Rohde & Schwarz SME signal generator.

Mapping the Data into the Baseband Waveforms:

The next question is, "How do we generate the baseband waveforms $c_I(t)$ and $c_Q(t)$?" There is no general answer to this question, as the generation of the baseband waveforms depends on the type of modulation. The following short descriptions will suffice for the moment.

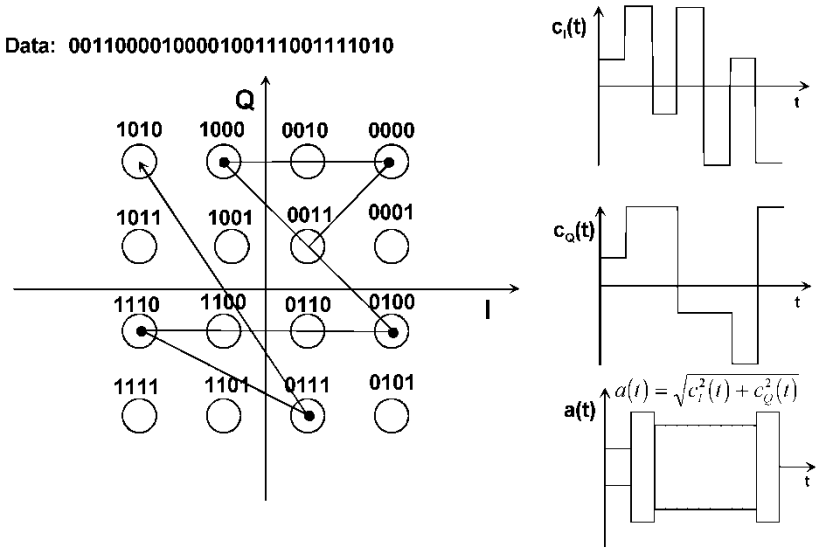


Figure 93: Constellation diagram, and baseband and RF signals of 16 QAM [1]

Linear modulations (all kinds of amplitude and phase-shift keying, and *M*-ary QAM):

- For binary amplitude and phase shift keying (ASK and BPSK), the data signal itself represented as a unipolar (ASK) or bipolar (BPSK) non-return-to-zero (NRZ) signal is the baseband waveform $c_I(t)$; the component $c_Q(t)$ does not exist.
- For *M*-ary phase shift keying and *M*-ary quadrature amplitude modulation, *N* bits are combined to form new symbols that are elements of an alphabet with $M = 2N$ elements. In the simplest case, every symbol is allocated an I and a Q amplitude during the symbol duration, which is *N* times the bit duration. The modulating signals $c_I(t)$ and $c_Q(t)$ are then staircase functions, and the modulated carrier has a time-varying envelope with the instantaneous amplitude $a(t)$ (Figure 93). Because the steps of the envelope cause unwanted side lobes of the RF spectrum, the baseband signals are filtered to smooth the shape of the RF envelope and reduce the occupied bandwidth of the modulated RF signal.
- Nonlinear modulations (frequency-shift keying, minimum shift keying and Gaussian minimum shift keying):
- Despite *M*-ary frequency shift keying (FSK) could be performed using I/Q modulator, for this type of modulation much simpler equipment such as a voltage controlled oscillator is used as a

frequency modulator. Figure 94 shows an example of quaternary frequency shift keying (4FSK), which also is known as 4 PAM/FM. This term indicates that every two bits are combined to make a dibit that is mapped into a baseband pulse with an amplitude taking on one of four possible levels. The pulse than is shaped by a base band filter before being fed to the frequency modulator.

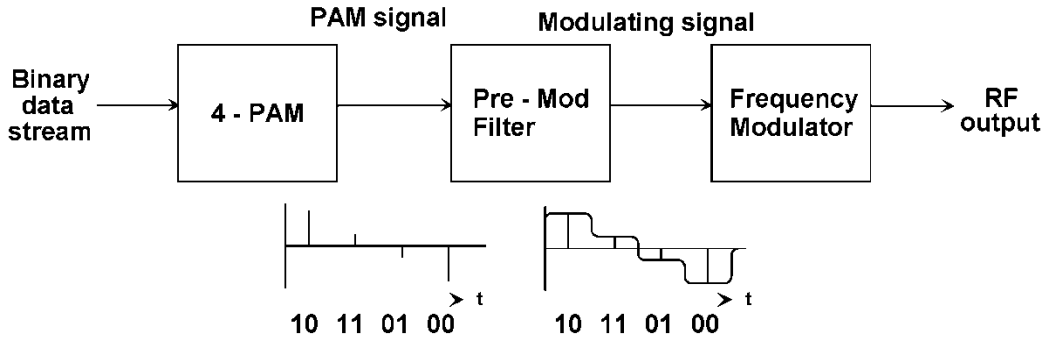


Figure 94: 4PAM/FSK [1]

If more precise modulations are required (for example, MSK and GMSK, which also turn out to be frequency modulations), first the instantaneous phase of the modulated RF carrier is calculated from the data. The corresponding sine and cosine values that form the modulating baseband signals $c_I(t)$ and $c_Q(t)$ are determined from a look-up table. This operation is the reason for the fact that frequency modulation is called a nonlinear modulation.

The Spectrum of a Digitally Modulated Carrier:

It is the task of any transmission process to occupy as little bandwidth as possible. The absolute lower limit in the baseband is half the symbol rate of the baseband signal, where for *M*-ary modulation the symbol rate r_{Symbol} is equal to the bit rate divided by *ld* (*M*). This lower limit is only theoretical as ideal rectangular filters which cannot be realized were necessary. Therefore, in practice, a minimum baseband bandwidth of about $0.75 r_{Symbol}$ has to be taken into account.

With linear modulation, the occupied bandwidth in the RF-range is twice the occupied baseband bandwidth. This follows from the lag theorem, according to which the double sided spectrum of a time function is shifted from $f = 0$ to the frequency $f = f_c$ when the time function is multiplied with $\cos(2\pi f_c t)$ (Figure 95).

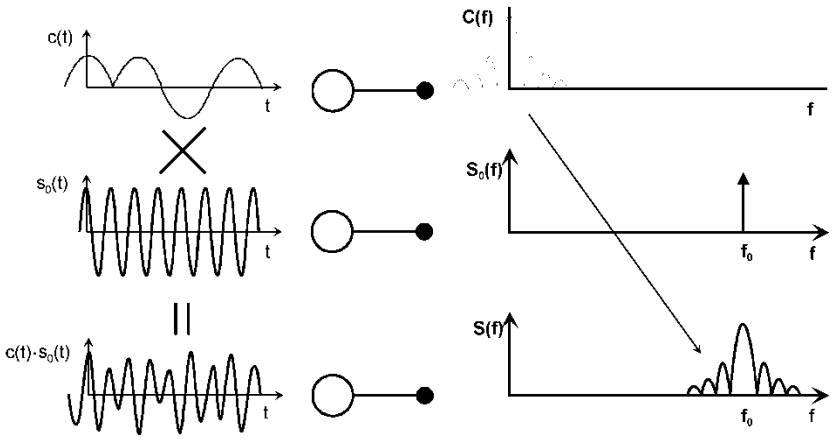


Figure 95: Occupied bandwidth in the baseband and the RF range [1]

Expressing this with formulas, we find:

$$c(t) \quad \circ\!\!-\!\!\bullet \quad C(f) \tag{42}$$

$$e^{j2\pi f_0 t}\, c(t) \quad \circ\!\!-\!\!\bullet \quad C(f - f_0) \tag{43}$$

Therefore, if the baseband spectrum is limited by a low-pass filter, the RF spectrum is limited as if it was filtered by an RF bandpass filter with twice the bandwidth of the baseband filter.

Putting it all together:

We started it all with an analog circuitry. The conventional recommendation is, unless a YIG oscillator is used, don't build a VCO above 6GHz. Why? The Figure of Merit (FOM) 'Q' of resonators and tuning diodes deteriorates rapidly, more aggressive than the 6dB/Octave noise increase. This is mostly due to the effect of the parasitic components and difficulties with the planar structure of transmission lines, maintaining 50Ω and once an inductor is reduced to 2 turns, the concentration of the magnetic field is not significant and the 'Q' suffers. Remember the best 'Q' is obtained if length/diameter ratio is more than 3, better 5. Therefore, it is better to multiply the 6GHz oscillator than to build one at 12GHz. See the paragraph about the push-push oscillator (pp-26). The block diagram below can use a mostly DDS based synthesizer. This would require a clock frequency of 12GHz. This is the current state-of-the-art possible in development stage.

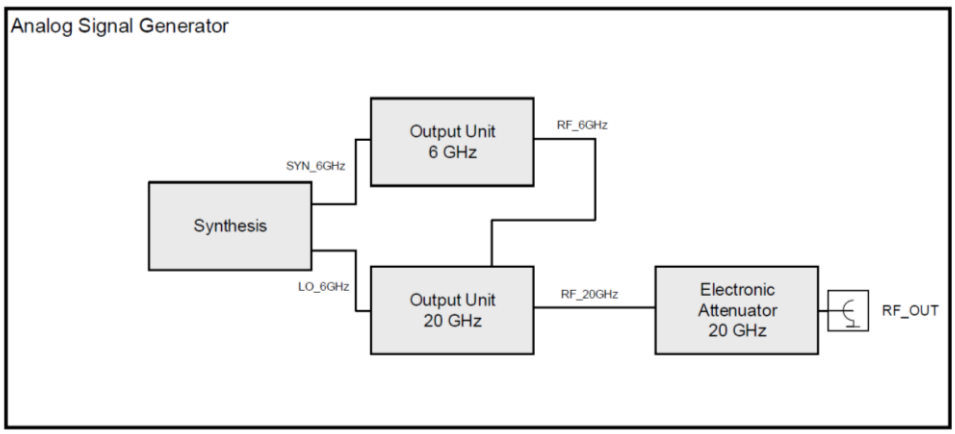


Figure 96: Analog Signal Generator (R&S)

The digital implementation requires the baseband generator which can be part of the IC and the I/Q modulator. So far I/Q modulators upto a bandwidth of 2GHz and more, have been implemented. The following block diagram shows such an implementation. To compensate frequency and temeprature dependence and drift, a complicated compensation circuit has to be in place.

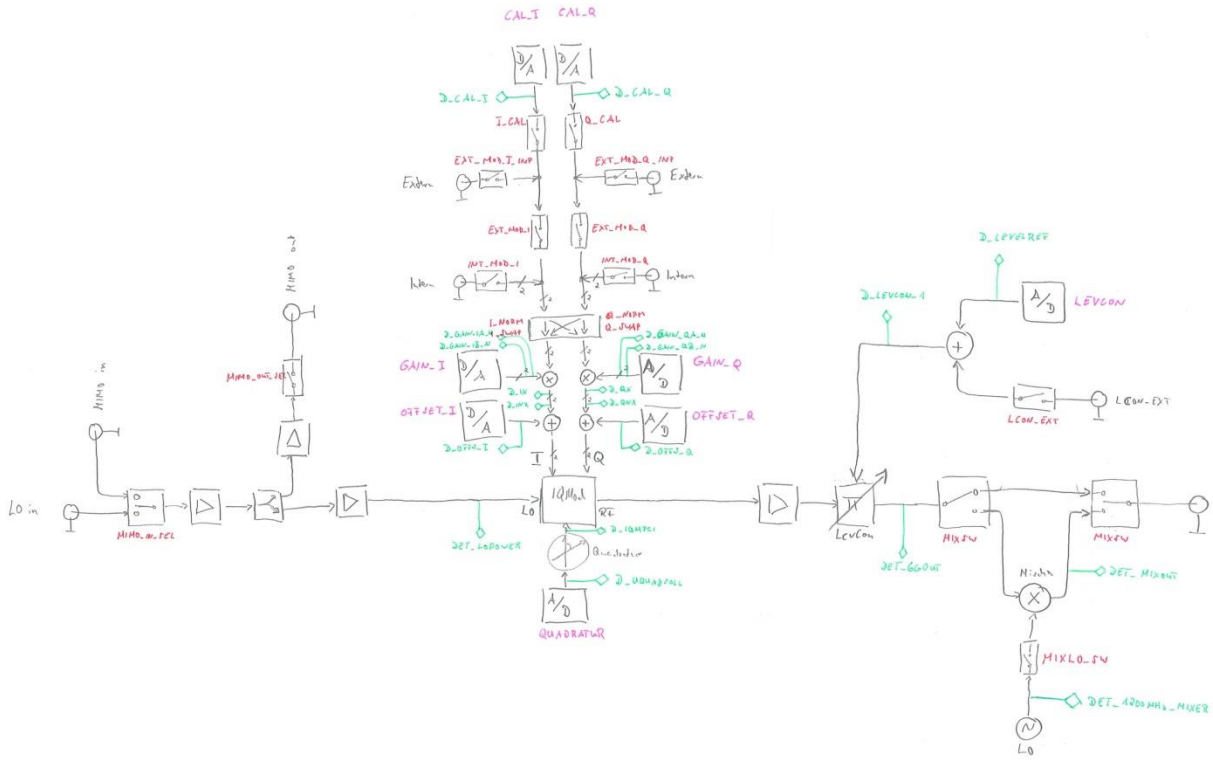
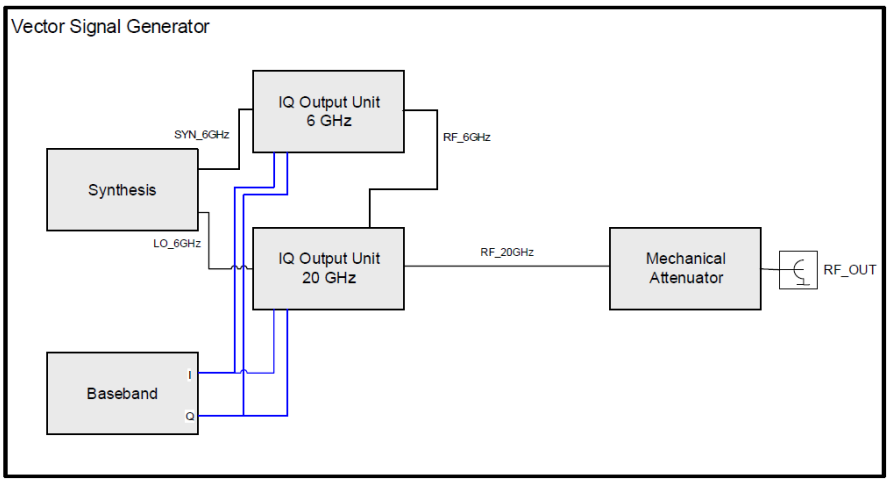


Figure 97: Implementation of an I/Q Modulator (R&S)



In addition to Analog Signal Generators, Vector Signal Generators include a Digital Baseband, which is connected to the Output Units, where we perform the IQ Modulation.

Figure 98: Vector Signal Generator (R&S)

The following are some block diagrams of signal generators which have been implemented.

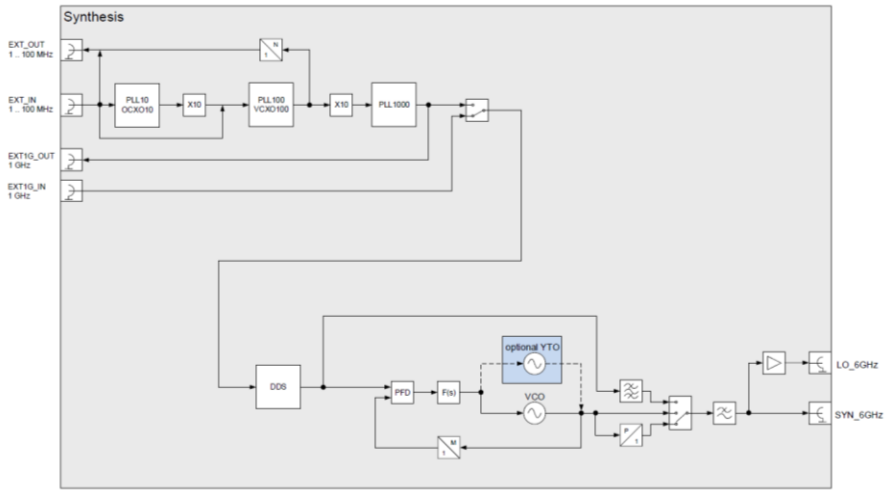


Figure 99: Synthesis (R&S)

The DDS on the lower part is triggered by a clock generator derived from a 1000MHz PLL. The DDS output which allows both arbitrary resolution as well as complex waveforms becomes the reference frequency for the PLL on its right side. Provisions for either a YIG oscillator or a VCO can be made. The switches allow choosing a suitable output frequency. This comparatively simple approach avoids the difficulties of a multi-loop synthesizer.

This only works well if a PLL system is available which accepts a 1GHz reference frequency. So far most PLLs avoid frequencies above 100MHz, as the phase-frequency discriminators are not fast enough.

20GHz Output Unit

On the 6 GHz Output Unit, we pass the signal through several amplifiers to achieve the desired power levels. The signal is then feed through a variable attenuator for AM modulation and level control. Most devices offer also a pulse modulator which completely mutes the RF signal. The optional IQ Modulator gives the possibility for Digital Modulation. At the end of the signal path, we find different Low Pass Filters for reducing the harmonic distortion and a level detector for the Automatic Level Control (ALC).

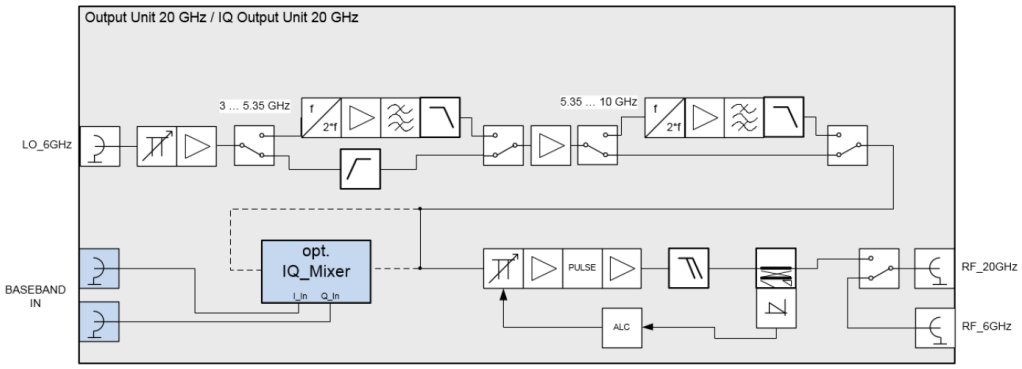


Figure 100: Output Unit 20GHz/IQ Output Unit 20GHz (R&S)

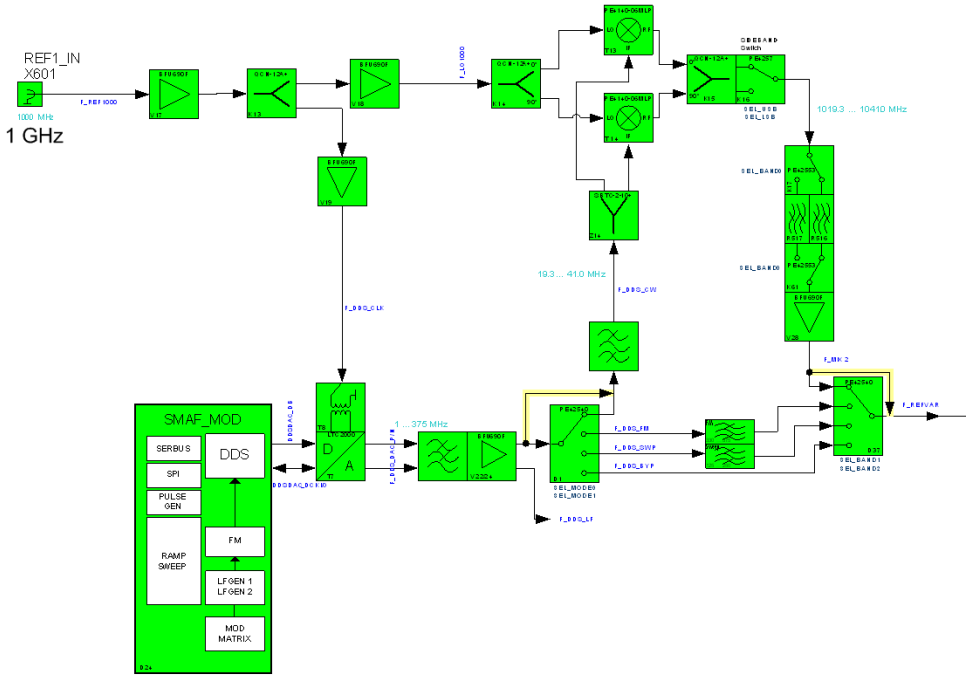


Figure 101: Variable Reference Modulation (R&S)

Now some applications and examples:

Figure 102: Smart Phones - a highly sophisticated SDR which is the most used application

A Further Example, Measurement of Military Radios

Radios used for aerospace and defense military communications – which will include air traffic control (ATC) systems for the purposes of this white paper – face a variety of challenges. In professional and security applications, the most stringent requirements are placed on characteristics such as availability, security and robustness. Users have become accustomed to small, trendy mobile phones with high data rates and modern design (gadgets) from the consumer driven market.

The requirements for military communications vary depending on the application. Conventionally, communications takes place in the frequency band from 1.5 MHz to 400 MHz and thus includes the HF, VHF and UHF bands and higher frequencies are being added.

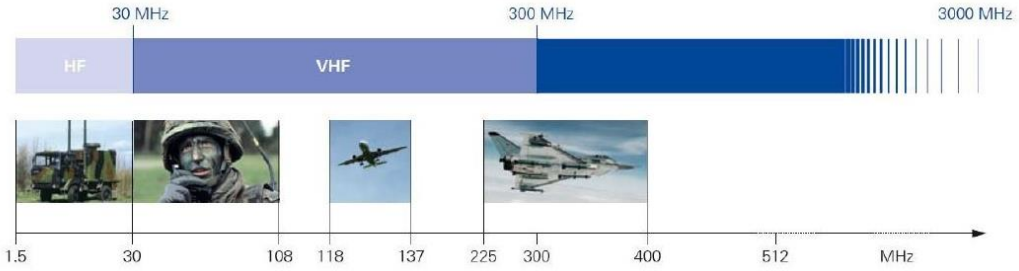
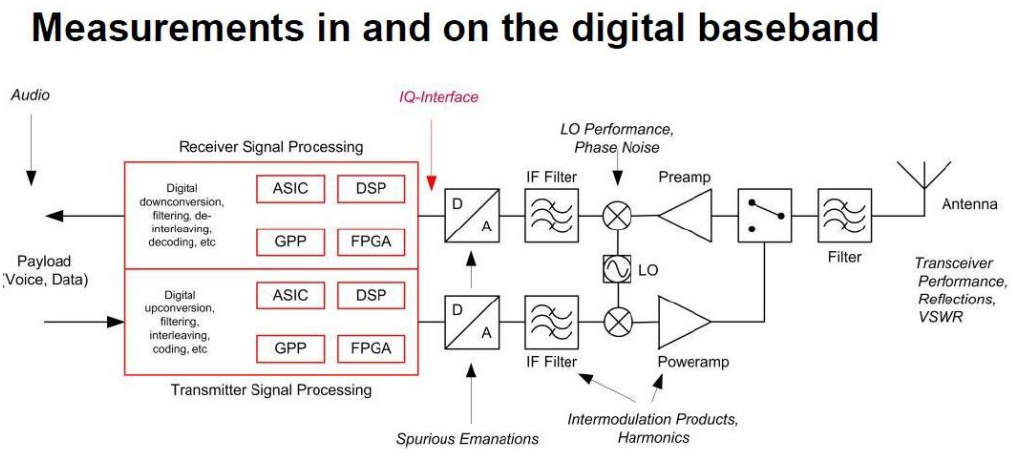


Figure 103: Frequency Bands for most Military Applications (R&S)

The following is a block diagram of a SDR and possible measurements.



The digital baseband module consists of several processors, including General Purpose Processors, DSPs and FPGAs, the associated storage medium, such as flash and/or DDR-RAM, as well as the internal communications buses between the individual components. Added to these are the external interfaces, such as an audio interface or a LAN connection, as well as a digital I/Q interface and low-speed control bus for connection to the TRX module.

Figure 104: Measurements in and on the digital baseband (R&S)

For cases where multi-tone signal test requirements exist, here is a 4-tone independent frequency synthesizer based on an IC by Texas Instruments, the DAC3xJ84 Quad-Channel, 16-Bit, 1.6/2.5 GSPS, Digital-to-Analog Converters with 12.5 Gbps JESD204B Interface.

Functional Block Diagram

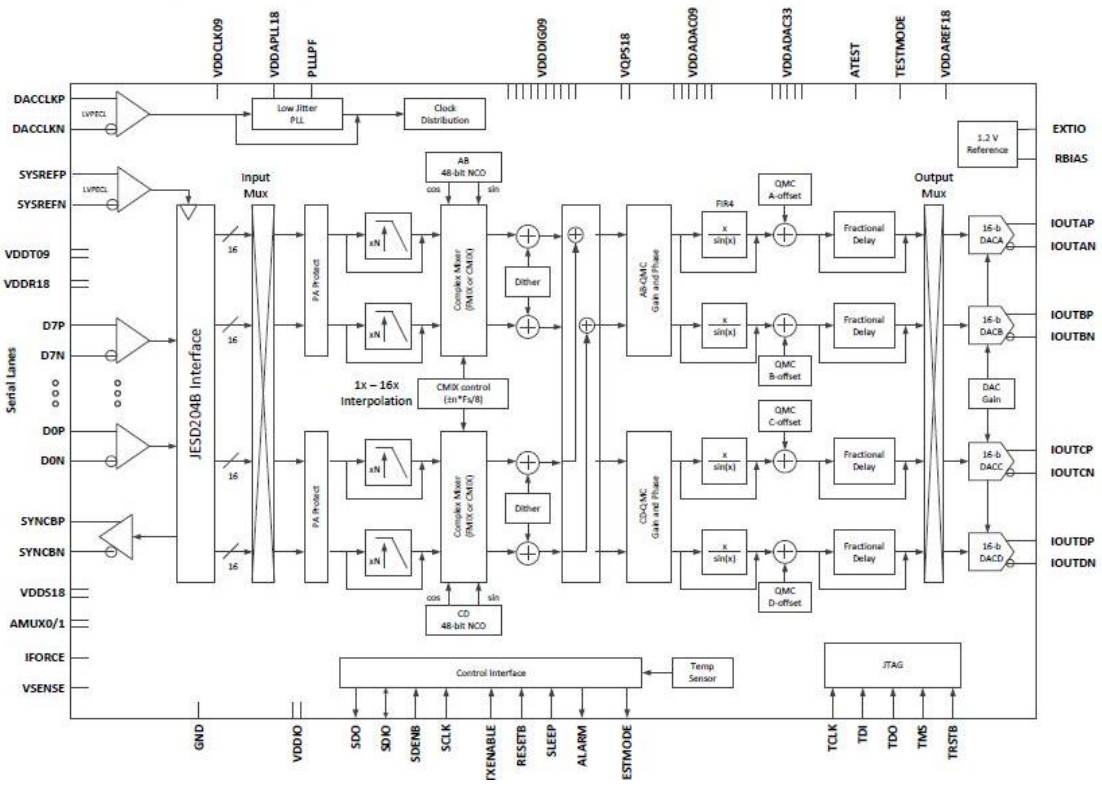


Figure 105: Texas Instruments – DAC3xJ84 [14]

Finally, here is the latest member of the family of radio testers, which uses all the exciting technologies as discussed above.

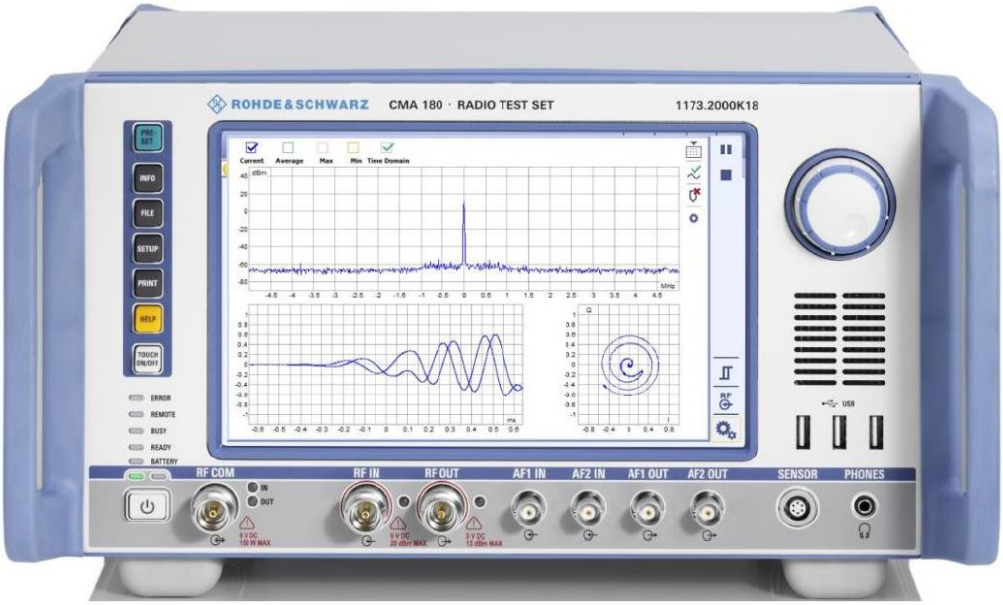


Figure 106: CMA Radio Test Set

Acknowledgement:

This presentation uses material back from 1965 to today, based on contributions from my friends and collegues at Rohde and Schwarz (Germany), Synergy Microwave Corp. (USA) and other companies like Analog Devices and Texas Instrumements and uses properly referenced material from published books on this topic. I hope I have personally thanked all friends and collegues who contributed to this lenghty summary paper. I am sure it will stay in flux and may require an update from time to time. If I have forgotten to reference someone or their material, I would like to apologize as a precaution, no harm intended.

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