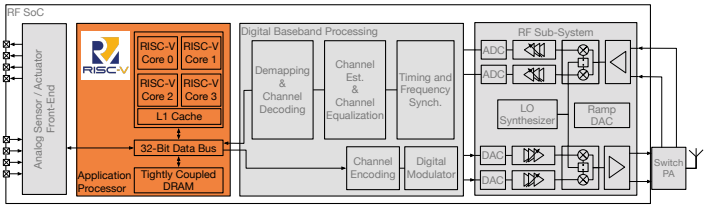
Chair of
„Secure Digital Circuits“

der Bundeswehr Universität München

Design of a RISC-V-based SoC Development Platform for IoT Communication Systems

Introduction



The Internet-of-Things (IoT) will feature a variety of new applications ranging from low-cost, low-complexity sensor nodes to ultra-reliable low-latency car-2-car communication links. The highly use-case specific requirements demand for a flexible design framework that allows to adapt a generic modem System-on-Chip architecture towards the different specifications.

Short Project Description

In this project, the groundwork towards such a flexible design framework shall be laid by realizing a scalable RISC-V-based processor cluster which can host the user application, the protocol software stack, and eventually part of the digital base-band algorithms. The integration of a first dedicated accelerator in hardware and software as well as mapping the processor cluster onto a Field Programmable Gate Array (FPGA) will serve as proof-of-concept at the end of this project.

Prerequisites

- Interest in processor design
- Experience in Hardware Description Languages (VHDL / Verilog) is helpful

What you will learn

You will gain insights in state-of-the-art processor architectures and get on-hand experience in modern embedded system design.

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