Topic

High-voltage RF switches in dedicated RF-CMOS-Switch technology for next generation mobile handheld devices

Description

High voltage linear RF switches implemented in dedicated bulk RF-CMOS technologies are operating at frequencies between 500 MHz and 6 GHz handling RF signals with voltage amplitudes of up to 80 V. These switches are primarily targeting antenna tuning application in mobile handheld devices. They are used to switch reactive components (inductors and capacitors) at the feed and aperture points of integrated antennas to reduce mismatch loss and improve radiation efficiency for various use conditions.

The scope of work spans over the three fields of expertize:

1) integrated *circuit design*, including RF design as a core and analogue/mixed-signal design as a supporting function for the core. The required EDA software tools include Cadence IC design environment, Keysight ADS, Ansys HFSS/Designer etc.

2) deep understanding of *physics* of the MOSFET switch device, close cooperation with technology development team;

3) *application* of high-voltage RF switches, including, but not limited to, antenna tuning in the mobile handheld devices.

Goals

1) Design of high voltage (80 V or higher) RF switches with best product-level FOM in already available and next-generation bulk RF-CMOS switch technologies;

2) Improve (optimize) design methodology for high-voltage RF switch products;

3) Propose novel switch structures addressing application needs, explore new application space.

Confidentiality

Some aspects of research work, especially related to technology development and particular aspects of physics of MOSFET switch devices, may be restricted for public disclosure. Innovative research results promising for utilization in the products may be protected by patents.

Publications

Target 2 conference papers per year (preferably, but not necessarily, one inter-continental and one local/European conference), 1 journal paper at the end.

Only results which are not falling into the “confidential” category will be published. Publishable results may include, for example, application-related ideas, novel ideas on the circuit design level with pure academic potential, solutions with supporting (not core) functions etc. Some innovative ideas may need to be patented before publication.

Duration

The target duration of the PHD work is 3 years

Research Environment

The work will be done at Infineon premises in Campeon in close cooperation with design, technology development and application teams. The supervisor at Infineon will be Valentyn Solomko.

Univ.-Prof. Dr. Linus Maurer
Universität der Bundeswehr
Institut für Mikroelektronik und Schaltungstechnik, EIT4
Werner-Heisenberg-Weg 39
D-85577 Neubiberg
Telefon: +49-(0)89-6004-3735
Mobil: +49 (172) 3867738
Fax: +49-(0)89-6004-2223
E-Mail: linus.maurer@unibw.de